CBCS SCHEME

USN | | | | | | | | | | |

15MT36

Third Semester B.E. Degree Examination, July/August 2022
Computer Organization

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain the Basic Operational concepts between the Processor and Memory. **(08 Marks)**

b. How to measure the performance of the Computer using Performance equation? **(08 Marks)**

OR

2 a. Explain the following instruction with example : i) MOVE LOC, R1 ii) ADD A, B, C iii) STORE R_i, A iv) LOAD A, R_6 v) SUBTRACT$(R1)_1$+ R5. **(10 Marks)**

b. Explain BIG-ENDIAN and LITTLE – ENDIAN methods with example. **(06 Marks)**

Module-2

3 a. Explain with example the following addressing modes :
i) Indirect mode ii) Indexing mode iii) Absolute mode. **(08 Marks)**

b. Explain Shift and Rotate instruction with example. **(08 Marks)**

OR

4 a. Explain the format of IEEE standard for floating point number. Also explain how normalization in IEEE is carried out. **(08 Marks)**

b. Discuss the following in case of subroutine :
i) Subroutine nesting ii) Parameter passing. **(08 Marks)**

Module-3

5 a. Describe the arrangement for Bus Arbitration using a Centralized and Distributed Arbitration. **(10 Marks)**

b. What is DMA? Explain the registers in a DMA interface. **(06 Marks)**

OR

6 a. With a block, describe a general 8-bit Parallel Interface. **(08 Marks)**

b. Describe Architecture and Protocols with respect to USB. **(08 Marks)**

Module-4

7 a. Analyze the Internal Organization of a 2M × 8 (16M) DRAM Chip. **(08 Marks)**

b. Explain the working of a CMOS memory cell. **(08 Marks)**

OR

8 a. What is a Cache? Explain any two Cache mapping functions with neat sketches. **(10 Marks)**

b. Define : i) Memory latency ii) Hit – rate iii) Miss penalty. **(06 Marks)**

Module-5

9 a. List the Control sequence for execution of Add (R3), R1 instruction. **(07 Marks)**

b. Explain with neat block diagram, Single – Bus Organisation of the data path inside a processor. **(09 Marks)**

OR

10 a. Discuss Microinstruction Sequencing Organization in Micro Programmed Control Unit. **(06 Marks)**

b. Explain with neat sketch, Hardwired Control Unit Organization. **(06 Marks)**

c. List the Action needed to execute the Instruction MOV (R1), R2. **(04 Marks)**

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