CBCS SCHEME

USN | | | | | | | | | | |

15EC63

Sixth Semester B.E. Degree Examination, July/August 2022
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Derive an expression for I-V characteristics with neat diagram. **(10 Marks)**

b. Explain pseudo nMOS inverter and derive the dc characteristics graphically. **(06 Marks)**

OR

2 a. Explain the steps of n-well CMOS fabrication process with neat diagrams. **(10 Marks)**

b. Explain any two non-ideal IV effects in a MOSFET. **(06 Marks)**

Module-2

3 a. Illustrate the schematic, stick diagram and layout for the Boolean expression $Y = \overline{(A + BC)}$ (Implement using CMOS logic) **(10 Marks)**

b. Define standard unit of capacitance. Calculate the standard value of capacitance for MOS transistor in 5 μm, 2 μm and 1.2 μm technologies. Given
gate capacitance for 5 μm = 4×10^{-4} pF/μm^2 ,
gate capacitance for 2 μm = 8×10^{-4} pF/μm^2 ,
gate capacitance for 1.2 μm = 16×10^{-4} pF/μm^2. **(06 Marks)**

OR

4 a. Derive an expression for the estimation of CMOS rise time delay and fall time delay. **(08 Marks)**

b. Explain the λ-based design rules for CMOS technology with neat diagrams. **(08 Marks)**

Module-3

5 a. Find the scaling factors for :
(i) Saturation current
(ii) Current density
(iii) Power dissipation/unit area
(iv) Maximum operating frequency. **(08 Marks)**

b. Describe Manchester carry-chain adder element. **(08 Marks)**

OR

6 a. Discuss the different bus architectures. **(08 Marks)**

b. With a neat diagram explain 4 × 4 Barrel shifter. **(08 Marks)**

Module-4

7 a. Realize NAND and NOR gate using Dynamic CMOS logic and explain its operation. **(08 Marks)**

b. Explain the 4-way data selector (multiplexer) with Boolean equation and nMOS based stick diagram. **(08 Marks)**

OR

8 a. Explain parity generator with the nMOS implementation of parity generator with stick diagram. **(08 Marks)**

b. Explain in detail the Generic Structure of FPGA architecture. **(08 Marks)**

Module-5

9 a. Explain 3-transistor dynamic RAM cell with neat diagram. **(08 Marks)**

b. Explain stuck at fault model in combinational circuits. **(08 Marks)**

OR

10 a. Demonstrate write operation and read operation for four transistor dynamic CMOS memory cell. **(08 Marks)**

b. Write a note on logic verification. **(08 Marks)**

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