CBCS SCHEME

USN | | | | | | | | | | |

17EC53

Fifth Semester B.E. Degree Examination, July/August 2022
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With a neat flow diagram, explain a typical design flow for designing VLSI IC circuits. **(08 Marks)**

b. Describe the digital system design using design hierarchy for 4-bit ripple carry counter. Write verilog code for the same. **(12 Marks)**

OR

2 a. With necessary blocks, explain the components of a simulation. **(06 Marks)**

b. Discuss the importance of HDL's. **(06 Marks)**

c. Define modules and instances. Describe four different description styles of verilog HDL. **(08 Marks)**

Module-2

3 a. Explain different data types of verilog HDL with examples. **(10 Marks)**

b. With an example of SR-latch, explain components of a verilog module. **(10 Marks)**

OR

4 a. What are system task and compiler directive? Explain in brief. **(10 Marks)**

b. Explain design hierarchical names for SR-latch simulation. **(10 Marks)**

Module-3

5 a. Write a verilog gate-level description for 4 to 1 multiplexer with logic diagram. **(10 Marks)**

b. With an example, explain the following operators:
(i) Reduction operators
(ii) Concatenation operator
(iii) Shift operators
(iv) Replication operator
(v) Conditional operator. **(10 Marks)**

OR

6 a. Write a verilog code for 4-bit full adder using dataflow operators. Also write stimulus for the same. **(10 Marks)**

b. Explain different types of gate delays with delay specification. **(10 Marks)**

Module-4

7 a. Explain Blocking assignments and Non-blocking assignments in verilog HDL. **(10 Marks)**

b. Explain the types of event-based timing control in verilog HDL. **(10 Marks)**

OR

8 a. Discuss the sequential and parallel blocks of verilog HDL. **(08 Marks)**

b. Write a verilog code for 4-to-1 multiplexer with case statement. **(06 Marks)**

c. With an example explain the following :
(i) Regular Delay control
(ii) Intra-assignment delay control
(iii) Level-Sensitive timing control **(06 Marks)**

Module-5

9 a. Describe a VHDL for design synthesis. **(12 Marks)**
b. Explain the data objects in VHDL. **(08 Marks)**

OR

10 a. Explain the different types of data types in VHDL. **(10 Marks)**
b. Write a VHDL code for 2-bit comparator using behavioral description. **(10 Marks)**

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