CBCS SCHEME

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17EC33

Third Semester B.E. Degree Examination, July/August 2022
Analog Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Starting from fundamentals, obtain the re model of BJT. **(04 Marks)**
   b. For a common emitter amplifier with fixed bias, derive the expressions for voltage gain input impedance and output impedance using re model. **(08 Marks)**
   c. Draw the circuit of common emitter amplifier with voltage divide bias configuration without emitter by-pass capacitor and calculate voltage gain, input and output impedances. The circuit parameters are $V_{CC} = 10$ V, $R_1 = 83$ KΩ, $R_2 = 17$ KΩ, $R_E = 1$ KΩ, $R_C = 2$ KΩ. Take $\beta = 100$. **(08 Marks)**

OR

2 a. Draw the circuit of emitter follower with voltage divider bias using h-parameter model. Derive the expressions for current gain, voltage gain input and output impedance. Use approximate h-parameter model. **(10 Marks)**
   b. For a BJT transistor, draw the circuit of hybrid-π model for common emitter configuration and explain the various parameters. **(10 Marks)**

Module-2

3 a. With the help of neat diagrams, explain the construction, working and characteristics of n-channel depletion MOSFET. **(08 Marks)**
   b. Draw the circuit of common source amplifier with bypass capacitor at the source terminal. Derive the expression for voltage gain and output impedance. **(08 Marks)**
   c. A common source amplifier with bypass capacitor has $R_D = 2$ KΩ, $R_S = 1$ KΩ, $R_G = 1$ MΩ, $g_m = 2$ m℧. Find voltage gain and output impedance. **(04 Marks)**

OR

4 a. Draw the circuit of common gate amplifier using JFET and derive the expressions for voltage gain, input and output impedances. **(10 Marks)**
   b. A common drain amplifier using JFET has the following circuit parameters $R_D = 2$ KΩ, $R_S = 1$ KΩ, $R_G = 1$ MΩ. Draw the amplifier circuit. The JFET has $I_{DSS} = 10$ mA, $V_P = -4$ V. Calculate g_m, voltage gain and output impedance. Take $V_{GS} = -2.4$ V. **(10 Marks)**

Module-3

5 a. Derive the expression for lower cut-off frequency and hence explain why gain decreases at lower and upper side of the frequency response of a BJT amplifier. **(10 Marks)**

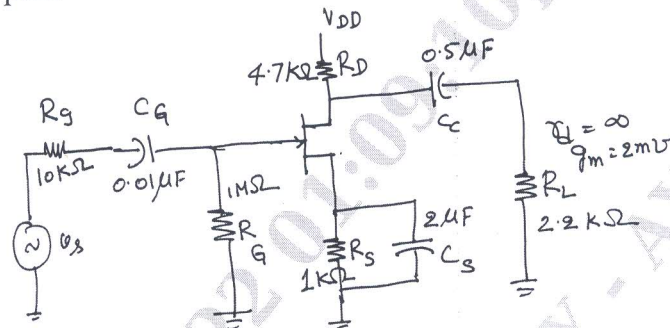b. For the following circuit [Fig.Q5(b)] find the lower cutoff frequency and sketch the frequency response plot.

Fig.Q5(b)

(10 Marks)

OR

6 a. Explain the miller capacitance and derive the expressions for miller capacitance at the input and output. (10 Marks)

b. With the help of suitable derivation, explain the effect of cascading the amplifier on the frequency response. (10 Marks)

Module-4

7 a. Draw the block diagram of voltage series feedback amplifier and derive the expression for input and output impedances. Comment on the effect of feedback on input and output impedances. (10 Marks)

b. Three identical amplifiers are cascaded. The open loop gain of each amplifier is subjected to variation 10% due to changes the supply voltage and working temperature with this cascaded amplifier, a feedback amplifier is to be designed so that the closed loop gain of the amplifier is $150 \pm 1\%$. Calculate the feedback factor required and open loop gain of each stage of the cascaded amplifier. (06 Marks)

c. State the merits of negative feedback in amplifiers. (04 Marks)

OR

8 a. Draw the circuit of Wien bridge oscillator and derive the expression for frequency of oscillation. Also explain the circuit connections. (08 Marks)

b. Draw the circuit of phase shift oscillator using JFET and explain its operation. Also write the expression for frequency of oscillation. (08 Marks)

c. Design a UJT oscillator for the following specification: $V_{BB} = 10$ V, $\eta = 0.7$, $V_V = 1$ V, $I_P = 10$ μA, $I_V = 1$ mA. (04 Marks)

Module-5

9 a. Draw the circuit of transformer coupled class-A amplifier and derive the expression for maximum efficiency. (10 Marks)

b. With the help of neat circuit diagram, explain operation of class B push pull amplifier and show that the maximum efficiency of the amplifier is 78.5%. (10 Marks)

OR

10 a. With the help of a block diagram, explain the series voltage regulator and also explain how the same can be implemented using BJT. (08 Marks)

b. A series voltagulator using BJT has $V_i = 20$ V, $R = 220$ Ω, $V_Z = 12$ V. Take $\beta = 50$. Find output voltage and output current for a load resistance of 500 Ω. Also find current through R. (06 Marks)

c. Explain the effect of harmonic distortion. Define harmonic distortion and total harmonic distortion. (06 Marks)

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