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15CS72

Seventh Semester B.E. Degree Examination, July/August 2022
Advanced Computer Architecture

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. With neat sketches, explain the Flynn's classification of computer architecture. **(06 Marks)**

b. With a neat diagram, explain different types of shared memory multiprocessor models. **(10 Marks)**

OR

2 a. Explain the different levels of parallelism in program execution on modern computers. **(08 Marks)**

b. For the following coarse-grain program graph with two processor p_1 and p_2. [Refer Fig.Q2(b)]

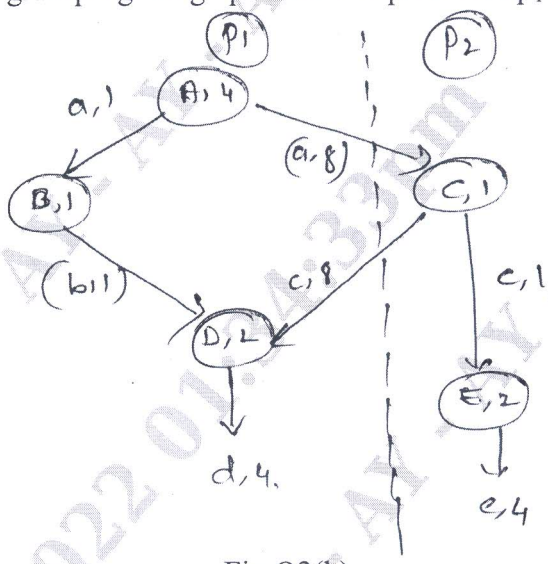

Fig.Q2(b)

Draw the following:
(i) Schedule chart without node duplication
(ii) Coarse-grain graph with node duplication.
(iii) Schedule chart with node duplication. **(08 Marks)**

Module-2

3 a. Explain the concept of instruction pipeline and also define basic definitions associated with instruction pipeline operations. **(08 Marks)**

b. Draw the neat sketch of a typical superscalar RISC processor architecture consisting of an integer unit and floating point unit. Also discuss the pipelining in super scalar processor. **(08 Marks)**

OR

4 a. With a neat diagram, explain the four levels of memory hierarchy. **(08 Marks)**

b. Explain the concept of address translation mechanism using TLB and various forms of page table. **(08 Marks)**

Module-3

5 a. With a neat diagram, explain the back plane bus specification, its interface and slot connections. **(08 Marks)**

b. Describe the sequential consistency model along with its necessary conditions to be satisfied. Also define 5 axioms for the same. **(08 Marks)**

OR

6 a. Explain the idea of internal data forwarding in pipeline. Also define three types of logic hazards which will affect out of order execution. **(08 Marks)**

b. With suitable examples, explain four types of block placement schemes for cache memory. **(08 Marks)**

Module-4

7 a. Explain the schematic design of a row of cross point switches in a cross bar network. **(08 Marks)**

b. With a proper illustration, explain snoopy bus protocol for cache coherence problem. **(08 Marks)**

OR

8 a. Explain different types of vector instructions along with diagrams. **(08 Marks)**

b. With a neat diagram, explain the concept of distributed shared memory with virtual memory mapping (SVM). **(08 Marks)**

Module-5

9 a. Describe four operational models used in programming multiprocessor systems. **(08 Marks)**

b. List out different language features set as a guidelines for developing user friendly programming environment. **(08 Marks)**

OR

10 Write short notes on:

a. Operand forwarding

b. Register renaming

c. Branch prediction

d. Reorder buffer **(16 Marks)**

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