CBCS SCHEME

17MT36

USN | | | | | | | | | |

Third Semester B.E. Degree Examination, Feb./Mar. 2022
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain with a neat timeline diagram how the user program and as routine share the processor for reading a machine level data and print the results. **(10 Marks)**
   b. Explain the basic operational concept between processor and memory. **(10 Marks)**

OR

2 a. Explain branching concept by considering example of adding "N" numbers using straight line program and using loop. **(10 Marks)**
   b. Explain the 2 ways that byte address can be assigned across word CBIG ENDIAN and LITTLE ENDIAN methods. **(10 Marks)**

Module-2

3 a. What are assembler directives? Explain assembler directives with example program. **(10 Marks)**
   b. What are addressing modes? Explain any 4 addressing modes. **(10 Marks)**

OR

4 a. What is stack and explain the operations of push and pop using instructions. **(10 Marks)**
   b. Explain subroutine with example. **(10 Marks)**

Module-3

5 a. What is direct memory access? Explain in detail. **(10 Marks)**
   b. Explain the steps used in enabling and disabling of interrupts. **(10 Marks)**

OR

6 a. What are interrupts? Explain the transfer of control through the use of interrupts. **(10 Marks)**
   b. Explain the steps involved in handling the interrupt from multiple devices. **(10 Marks)**

Module-4

7 a. Explain the operation of a synchronous DRAM using a neat diagram along with a burst read of length 4 in a SDRAM. **(10 Marks)**
   b. Draw the organization of 16×8 memory chip and explain its working. **(10 Marks)**

OR

8 a. Draw and explain the internal organization of the $2m \times 8$ dynamic memory chip. **(10 Marks)**
   b. What is virtual memory? Explain the virtual memory organization. **(10 Marks)**

Module-5

9 a. Explain the single bus organization of the data path inside a processor with a neat diagram. **(10 Marks)**
   b. Write the control sequence for conditional and unconditional branch instruction. **(10 Marks)**

OR

10 a. Write the control sequence for execution of the instruction add (R_3), R_1. **(10 Marks)**
    b. Explain the multiple bus organization of the data path with a neat diagram. **(10 Marks)**

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