CBCS SCHEME

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17MT35

Third Semester B.E. Degree Examination, Feb./Mar.2022
Analog & Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define filter. List and explain the classification of filters. Also mention the advantages of active filter over passive filter. **(10 Marks)**

b. With a neat sketch derive the expression for gain of a first order Butterworth high pass filter. Also draw the frequency response curve. **(10 Marks)**

OR

2 a. With a neat sketch demonstrate the operation of a narrow band reject filter and also write necessary equations with frequency response curve. **(10 Marks)**

b. Design a wide band pass filter with outoff frequencies 200 Hz and 1 kHz and a pass band gain of 4. Also plot frequency response curve and calculate Q factor. **(10 Marks)**

Module-2

3 a. Derive the condition for oscillation with a block diagram. Also define oscillator. **(10 Marks)**

b. With a neat circuit, illustrate the working of RC-phase shift oscillator with relevant equations. **(10 Marks)**

OR

4 a. With a neat circuit and input output waveform illustrate the working inverting comparator circuit. **(10 Marks)**

b. Demonstrate the working of Schmitt Trigger. With neat circuit diagram and input output waveform. **(10 Marks)**

Module-3

5 a. With a neat sketch, explain the block diagram of 555 Timer. **(10 Marks)**

b. With a neat sketch, explain the working of monostable multivibrator as frequency divider. **(10 Marks)**

OR

6 a. With a neat sketch, explain the working of 555 timer as Astable multivibrator. With relevant equations and waveforms. **(10 Marks)**

b. Explain the working of Astable multivibrator as Free running ramp generator. **(10 Marks)**

Module-4

7 a. Simplify the following Boolean function $F = \overline{A}C + \overline{A}B + A\overline{B}C + BC$ using K map and also illustrate NAND and NOR gate realization of it. **(10 Marks)**

b. Design a BCD to decimal decoder. **(10 Marks)**

OR

8 a. Define MUX, Design a 4×1 multiplexer. Also implement the Boolean function $F(A,B,C)=\sum(1,3,5,6)$ with a multiplexer. **(10 Marks)**

b. With a neat circuit, illustrate the working of 2 to 4 line decoder. Also design a 4×16 decoder using 3×8 decoder. **(10 Marks)**

Module-5

9 a. Derive the characteristic equation for the following. Also write circuit and characteristic table:
   (i) SR flip flop.
   (ii) D flip flop. **(12 Marks)**

b. Design a 3 bit synchronous binary us counter.. **(08 Marks)**

OR

10 a. Design a BCD ripple counter. **(12 Marks)**

b. Design a 3 bit binary ripple down counter. **(08 Marks)**

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