CBCS SCHEME

USN | | | | | | | | | | |

15MT36

Third Semester B.E. Degree Examination, Feb./Mar. 2022
Computer Organization

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the basic operational concepts between the processor and memory. **(08 Marks)**

b. How to measure the performance of the computer using performance equation? **(08 Marks)**

OR

2 a. Explain the following instruction with example :
i) MOVE LOC, R1 ii) ADD A, B, C iii) STORE R_i, A
iv) LOAD A, R_6 v) SUBTRACT$(R1)_1$+ R5 **(10 Marks)**

b. Explain BIG-ENDIAN and LITTLE – ENDIAN methods with example. **(06 Marks)**

Module-2

3 a. Define addressing mode and explain any 4 addressing modes with example. **(10 Marks)**

b. What is subroutine linkage? With example explain passing parameters to subroutine. **(06 Marks)**

OR

4 a. What is stack frame? Explain commonly used layout for information in a subroutine stack frame. **(10 Marks)**

b. Explain different logical and arithmetic shaft operations. **(06 Marks)**

Module-3

5 a. Define memory mapped I/O and I/O mapped I/O with example. **(04 Marks)**

b. Explain how interrupt request from several I/O devices can be communicated to a processor through a single INTR line. **(04 Marks)**

c. Describe DMA concept in brief. **(08 Marks)**

OR

6 a. Define bus arbitration. Explain in detail any one approach of bus arbitration. **(08 Marks)**

b. Discuss briefly the protocols of USB. **(08 Marks)**

Module-4

7 a. Draw the circuit diagram of SRAM cell and DRAM and explain the read/write operation. **(05 Marks)**

b. Give the list of all possible non-volatile memory. **(03 Marks)**

c. Draw the block diagram of synchronous DRAMs and explain the operation with timing diagram. **(08 Marks)**

OR

8 a. The main memory size is 64 KB and cache memory size is 8 KB. Each memory is divided into the size of 1 KB module. Give the address mapping scheme using (i) direct mapping (ii) associative mapping. **(08 Marks)**

b. Draw the block diagram of virtual memory address translation method and explain how virtual address is converted into the physical address. **(08 Marks)**

Module-5

9 a. Draw the diagram of single-bus organization of the datapath inside a processor and explain the steps to execute an instruction. **(08 Marks)**

b. List the control sequences needed for the execution of an instruction add (R_2), R_1. **(08 Marks)**

OR

10 a. Draw the diagram of three bus organization of the datapath and write the control sequences needed to execute an instruction add R_1, R_2, R_3. **(08 Marks)**

b. Explain with diagram the operation of the microproframmed control unit. **(08 Marks)**

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