CBCS SCHEME

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18MT35

Third Semester B.E. Degree Examination, Feb./Mar. 2022
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define clipper construct a double ended clipper to clip the output at +3V and –2V from 10V (P – P) supply voltage. **(08 Marks)**

b. Define filter. Mention the advantages of active filters over passive filters. Also with a neat sketch explain the operation of first order active low pass filter and derive the expression for gain. **(12 Marks)**

OR

2 a. With a neat sketch, explain the operation of notch filter. Also mention its application. **(10 Marks)**

b. Design a wide band pass filter with cut off frequencies 200Hz and 1KHz and pass band gain = 4. Also calculate quality factor. **(10 Marks)**

Module-2

3 a. With the neat sketch and necessary equations explain the operation o RC – Phase shift oscillator. **(10 Marks)**

b. With a neat sketch explain the working of inventing comparator circuit. Plot the waveform for positive and –ve reference voltage. **(10 Marks)**

OR

4 a. Demonstrate the working of Schmitt trigger circuit with necessary equations and waveforms. Also draw hysteresis curve. **(10 Marks)**

b. With the neat sketch, explain the working of Wein bridge oscillator. **(10 Marks)**

Module-3

5 a. With the help of block diagram, explain the working of Astable multivibrator circuit : write necessary expressions and plot waveforms. **(12 Marks)**

b. Design a divide by 2 network for a frequency of input trigger signal 2KHz. **(08 Marks)**

OR

6 a. With the help of block diagram explain the working monostable multivibrator circuit with relevant equations and waveforms. **(12 Marks)**

b. With the neat sketch, explain how to construct a square wave generator from Astable multivibrator. **(08 Marks)**

Module-4

7 a. Simplify the following Boolean function in :
i) Sum of products
ii) Product of sums
iii) Also with the circuit
$F(A, B, C, D) = \Sigma(0, 1, 2, 3, 5, 8, 9, 10)$. **(12 Marks)**

b. Implement a full adder circuit from two half adder. **(08 Marks)**

OR

8 a. Define MUX, construct a 4 × 1 MUX. Also implement the following Boolean expression using MUX. **(12 Marks)**

b. Implement a full adder circuit using decoder IC. **(08 Marks)**

Module-5

9 a. With the neat circuit derive the characteristic equation for the following :
i) Clocked D flip-flop
ii) Clocked JK flip-flop. **(12 Marks)**

b. Design a 3 bit binary ripple up counter. **(08 Marks)**

OR

10 a. Implement a BCD ripple counter. **(12 Marks)**

b. Design a 3 bit synchronous binary up counter. **(08 Marks)**

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