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15EC63

Sixth Semester B.E. Degree Examination, Feb./Mar. 2022 **VLSI** Design

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 With neat diagrams, explain the operation of nMOS enhancement mode transistor. (06 Marks)
 - Explain the following non-ideal effects of MOS device
 - Channel length modulation
 - Body effect ii)
 - iii) Noise margin.

(10 Marks)

- 2 With neat diagrams, discuss the nMOS fabrication process steps. (08 Marks)
 - Explain the CMOS inverter DC characteristics with neat diagrams and equations. (08 Marks) b.

Module-2

- Draw the circuit diagram and stick diagram for the expression f = A(B+C) using nMOS and CMOS design styles.
 - With neat diagrams, explain λ-based design rules for wires, transistors and contacts in nMOS and CMOS process. (08 Marks)

OR

- Derive an equation for rise time and fall time with respect to CMOS inverter.
 - Estimate the total area capacitance for the structure shown in Fig.Q4(b). Consider 5µm technology with relative C values for metal = $0.075\Box Cg$ and polysilicon = $0.1\Box Cg$.

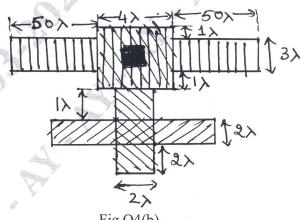


Fig.Q4(b)

(06 Marks)

Module-3

- 5 Identify various scaling models and derive the scaling factors for any eight device parameters. (10 Marks)
 - Explain the operation of 4-bit barallel shifter with neat diagram.

(06 Marks)

OR

- 6 a. Implement 4-bit carry look ahead adder using Multiple Output Domino Logic (MODL) with necessary equations.

 (08 Marks)
 - b. With neat circuit diagram and truth table, explain the operation of Manchester carry chain adder.

 (08 Marks)

Module-4

- 7 a. Explain the operation of (n + 1) bit parity generator with relevant circuit diagram and stick diagram. (08 Marks)
 - b. Implement 4:1 MUX using switch logic with relevant truth table and equations. Also write the stick diagram. (08 Marks)

OR

- 8 a. With neat diagram, explain design abstraction for FPGA (Filed Programmable Gate Array).
 (08 Marks)
 - b. Explain the architecture of field programmable gate array. (08 Marks)

Module-5

- 9 a. Explain the operation of 4 transistor dynamic memory and 6 transistor CMOS memory cells with sense amplifier circuit with neat circuit diagrams. (10 Marks)
 - b. Explain the operation of D-latch using nMOS and CMOS design styles. (06 Marks)

OR

- 10 a. Identify various fault models and explain each fault model with relevant diagrams and layout. (12 Marks)
 - b. Explain the operation of built in logic block observation (BILBO) used in testing. (04 Marks)
