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10EC56

Fifth Semester B.E. Degree Examination, Feb./Mar. 2022
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Compare CMSO and Bipolar technology. **(06 Marks)**
b. Describe in detail step-by-step procedure of P-well CMOS fabrication. **(07 Marks)**
c. Derive the expression for V_{out} in the B-Region of CMOS inverter. **(07 Marks)**

2 a. Define noise margin. Obtain the expression for of V_{IL}, V_{IH}, V_{OL} and V_{OH} form the transfer characteristic of a typical inverter. **(06 Marks)**
b. Draw the schematic, stick diagram and layout of CMOS design for the following Boolean expression $F = \overline{AB + E + CD}$. **(06 Marks)**
c. With neat diagram, explain λ - based design rules for wires (nMOS and CMOS). **(08 Marks)**

3 a. Realize 2 – input NAND gate for BiCMOS logic structure. **(05 Marks)**
b. Realize for $Z = \overline{A(B+C) + DE}$ for clocked CMOS logic structure. **(05 Marks)**
c. What are the properties of nMOS and PMOS pass transistor? How is transmission gate is useful. **(06 Marks)**
d. Draw the pass transistor logic for 2-inoput NAND and NOR gate. **(04 Marks)**

4 a. Derive an expression for rise time and fall time estimation. **(06 Marks)**
b. Explain inverting and non inverting nMOS super buffer. **(06 Marks)**
c. Discuss the effect of scaling in MOS circuit
i) Limits of miniaturation
ii) Limits of interconnects and contact resistance. **(08 Marks)**

PART – B

5 a. Discuss the architecture issues to be followed in the design of a VLSI subsystem. **(05 Marks)**
b. Explain Bus arbitration logic n-line bus with schematic and stick diagram. Also explain structure design. **(10 Marks)**
c. Explain 4-bit nMOS dynamic shift register with schematic and stick diagram. **(05 Marks)**

6 a. Explain the implementation of ALU function with a standard adder. **(10 Marks)**
b. With neat diagram, explain Braun array multiplier. **(10 Marks)**

7 a. Explain the CMOS pseudo static D – flip flop circuit. **(05 Marks)**

b. Explain with neat diagram of four transistor dynamic and six transistor static CMOS memory cell. **(08 Marks)**

c. Explain with neat diagram of Decoder based selection and control memory cell. **(07 Marks)**

8 a. Explain how to find minimum test vector to find fault in combinational circuit using sensitized path based testing. **(08 Marks)**

b. Explain with neat diagram of scan path testing technique. **(07 Marks)**

c. Explain linear feedback shift register to generate test vector in BIST. **(05 Marks)**

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