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17EC45

Fourth Semester B.E. Degree Examination, Feb./Mar. 2022
Linear Integrated Circuit

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Draw the internal block schematic of OP-Amp and explain. Also list the ideal characteristics of an Op – Amp. (06 Marks)
- b. Design Direct Coupled non - Inverting Amplifier using 741 IC. Let the voltage gain of Amplifier be approximately 100. The signal amplitude is to be 15mV. (07 Marks)
- c. With neat sketch, discuss the operation of 3 input inverting summing amplifier. And show that output is inverted sum of inputs. (07 Marks)

OR

- 2 a. A $1k\Omega$ load is to have 5V developed across it from a 15V source. Design a single power supply voltage follower circuit and calculate the load voltage variation in each case when the load resistance varies by -10%. Use a 741 Op-Amp. (07 Marks)
- b. With neat circuit diagram, explain the Operation of Difference Amplifier and show that output $V_o = (V_2 - V_1)$. (06 Marks)
- c. Design an direct coupled inverting amplifier using 741 Op-Amp. The voltage is to be 50 and the output voltage amplitude is to be 2.5V. (07 Marks)

Module-2

- 3 a. Discuss the operation of HIGH Z_{IN} capacitor coupled voltage follower with suitable diagram and write design procedure. (06 Marks)
- b. Design a capacitor coupled voltage follower using a LF353 BIFET Op-Amp. The lower cut-off frequency for the circuit is to be 50Hz and load resistance is $R_L = 3.9 k\Omega$. (07 Marks)
- c. With neat circuit diagram, explain the operation of Instrumentation Amplifier with necessary mathematical proof. (07 Marks)

OR

- 4 a. Explain the operation of Inverting precision half wave rectifier with neat circuit and waveforms. (06 Marks)
- b. Design a Capacitor Coupled Inverting amplifier for a pass band gain of 100, $f_1 = 120Hz$ and $f_2 = 5KHz$. Assume $R_L = 2K\Omega$ and use LF353 BIFET Op-Amp. (07 Marks)
- c. Explain how the upper cut – off frequency can be set for Inverting and non – Inverting amplifiers. (07 Marks)

Module-3

- 5 a. With neat circuit diagram and waveforms, explain detailed operation of Sample and Hold circuit. List the application of same. (06 Marks)
- b. With neat circuit diagram and waveforms, explain the operation of Inverting Schmitt trigger. (07 Marks)
- c. A capacitor coupled zero crossing detector is to provide an output voltage of approximately $\pm 17V$, when $3KHz$, $\pm 2V$ square wave Input is applied. Design a suitable circuit to use a bipolar Op-amp. (07 Marks)

OR

- 6 a. What are necessary conditions for generating Oscillations? Explain the operation of Wein bridge Oscillator. (06 Marks)
- b. Explain the operation of Log Amplifiers. (07 Marks)
- c. Design an Inverting Schmitt trigger circuit is to have $V_{UTP} = 0V$ and $V_{LTP} = 1V$. Design suitable circuit using a bipolar Op-Amp and $\pm 15V$ supply. (07 Marks)

Module-4

- 7 a. Mention the advantages of active filters and using 741 Op-amp design a first order active low pass filter to have a cut off frequency of 1KHz. (06 Marks)
- b. Design a Second order active high pass filter to have a cut off frequency of 12KHz. Use a 715 Op-amp. (07 Marks)
- c. With neat block diagram and necessary wave form construct Band elimination filter using LPF and HPF and explain. (07 Marks)

OR

- 8 a. With neat diagram, explain the operation of Series Op-amp regulator. (06 Marks)
- b. Explain the Standard representation / Configuration of 78XX and 79XX regulators. (07 Marks)
- c. List and explain the characteristics of 3 – terminal IC regulators. What are the advantages and disadvantages? (07 Marks)

Module-5

- 9 a. Draw the block diagram of PLL and explain and also list the application of PLL. (06 Marks)
- b. With neat diagram, explain the operation of Successive Approximation ADC. What are the drawback of it? (07 Marks)
- c. The basic step size of 4 – bit DAC is 312.5mV. If 0000 represents 0 V. Calculate the analog output voltage produced for the digital inputs : i) 1101 ii) 0111 iii) 1010. (07 Marks)

OR

- 10 a. Design a 555 Astable multi vibrator to operate at 5KHz with duty cycle of 40%. Sketch the designed circuit. (06 Marks)
- b. Design a Mostable Multivibrator using 555 Timer to obtain a pulse width of 10msec. (07 Marks)
- c. Explain the operation of 555 Timer as a Astable multivibrator using internal diagram of 555 block. (07Marks)

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