CBCS SCHEME

USN | | | | | | | | | | |

15EC46

Fourth Semester B.E. Degree Examination, Feb./Mar. 2022
Linear Integrated Circuits

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the basic op-amp circuit with necessary equations. **(08 Marks)**

b. Write a short note on :
i) CMRR ii) Slew Rate **(08 Marks)**

OR

2 a. Explain the difference amplifier circuit. Discuss the common mode nulling. **(08 Marks)**

b. Using 741 op-amp, design non-inverting amplifier to have voltage gain of approximately 66. The signal amplitude is to be 15mV. **(08 Marks)**

Module-2

3 a. Explain the capacitor coupled voltage follower with circuit diagram and equations. Design capacitor coupled voltage follower using 741 op-amp. The lower cut-off frequency for the circuit is to be 50Hz and the load resistance R_L is 3.9KΩ. **(10 Marks)**

b. Explain how the cut-off frequency (Upper cut-off frequency) can be set for inverting amplifier with neat circuit diagram. **(06 Marks)**

OR

4 a. Write a short note on :
i) Low Resistance Voltage Sources
ii) Current sinks. **(08 Marks)**

b. Design non-saturating precision half wave rectifier to produce 2V peak output from sine wave input with peak value of 0.5V and frequency of 1MHz. Use bipolar op-amp with supply voltage of ±15V. **(08 Marks)**

Module-3

5 a. Explain the peak clipper circuit with design equations. **(08 Marks)**

b. Explain the working of phase shift oscillator with circuit diagram, waveforms and equations. **(08 Marks)**

OR

6 a. Explain the operation of capacitor coupled zero crossing detector, with neat circuit diagram, waveforms and equations. **(08 Marks)**

b. Explain the antilog amplifier with neat circuit diagram and derive its output equation. **(08 Marks)**

Module-4

7 a. Explain the operation of first order active low pass filter with neat circuit diagram, frequency response and design steps. Using 741 op-amp, design first order active low pass filter to have cut-off frequency of 1KHz. **(08 Marks)**

b. Design single stage band pass filter to have voltage gain of 1 and passband from 300Hz to 30KHz. Assume $C_2 = 1000pf$. **(04 Marks)**

c. Explain how low pass filter and high pass filter are used as band-stop filter with block diagram and frequency response. **(04 Marks)**

OR

8 a. Explain :
i) A regulated power supply using discrete components
ii) Fixed regulator used as adjustable regulator
iii) With neat circuit diagrams. **(08 Marks)**

b. Explain the standard representation of 3 – terminal IC regulator with its characteristics. Also define line regulation and load regulation. **(08 Marks)**

Module-5

9 a. Explain digital phase detectors with necessary diagrams and waveforms. **(08 Marks)**

b. With neat block diagram, explain the operation of PLL. Define :
i) Lock in range ii) Capture range iii) pull in time. **(08 Marks)**

OR

10 a. Explain the operation of monostable multivibrator using 555 timer with internal diagram. **(08 Marks)**

b. Explain R – 2R ladder DAC with circuit diagram and equations. What output voltage would be produced by D/A converter whose output range is 0 to 10V and whose input binary number is
i) 10 (For 2 – bit D/A converter)
ii) 0110(For 4 – bit D/A converter). **(08 Marks)**

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