USN ☐☐☐☐☐☐☐☐☐☐   **10EC45**

Fourth Semester B.E. Degree Examination, Feb./Mar. 2022
Fundamentals of HDL

Time: 3 hrs.   Max. Marks:100

Note: *Answer any FIVE full questions, selecting at least TWO full questions from each part.*

PART – A

1   a. Discuss the various data types in verilog with examples.   **(12 Marks)**
    b. Explain data-flow description in VHDL and verilog using half adder as an example.
                                                                                    (08 Marks)

2   a. With a neat gate-level diagram of a 2 × 2 – bit combinational array multiplier, write its VHDL code.   **(10 Marks)**
    b. Write VHDL code of a 2 × 1 multiplexer with a logic diagram.   **(10 Marks)**

3   a. Write VHDL code behavioral description for a D-Latch using signal-assignment statements and sketch its simulation waveform. Also write the truth table.   **(12 Marks)**
    b. Write the structural VHDL description of a full adder with logic symbol and diagram.
                                                                                    (08 Marks)

4   a. What is the importance of binding in HDL? Explain binding between:
        i)   Entity and architecture in VHDL
        ii)   Entity and component in VHDL.   **(10 Marks)**
    b. Write the flow chart for booth algorithm and show the steps of booth algorithm taking X = 1011 and Y = 0111.   **(10 Marks)**

PART – B

5   a. Write VHDL and verilog code for a full adder using procedure and task. Also write the full adder circuit.   **(10 Marks)**
    b. Explain Mixed-Language description of a Master-Slave D flip-flop (write the circuit).
                                                                                    (10 Marks)

6   a. Write VHDL code for addition of two [5 × 5] matrices.   **(08 Marks)**
    b. Explain, invoking a VHDL entity from a verilog module and invoking a verilog module from a VHDL module.   **(12 Marks)**

7   a. Explain VHDL file processing with examples.   **(10 Marks)**
    b. Write declaration of VHDL single – dimensional arrays and verilog single-dimensional array.   **(04 Marks)**
    c. Write verilog code for finding the greatest element of an array.   **(06 Marks)**

8   a. Explain verilog synthesis information from module inputs/outputs.   **(08 Marks)**
    b. Explain mapping the loop statement with an example.   **(12 Marks)**

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