CBCS SCHEME

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17EC34

Third Semester B.E. Degree Examination, Feb./Mar. 2022
Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Write K-Map and list min terms and max terms for $y = f(a, b, c, d) = b + c\bar{d}$. **(04 Marks)**

b. Simplify using K-map and Implement using basic gates $P = f(v, w, x, y, z) = \sum m(0, 5, 7, 9, 15, 18, 21, 29, 30)$. **(08 Marks)**

c. Simplify using Quine McCluskey minimization technique
$R = f(l, m, n, o, p) = M_0 M_5 M_7 M_{10} M_{17} M_{22} M_{27} M_{30}$. **(08 Marks)**

OR

2 a. Simplify the function $f(d, e, f, g) = \sum m(0, 1, 2, 4, 5, 7, 9, 12)$ using K-map. **(04 Marks)**

b. $f(w, x, y, z) = \sum m(0, 1, 3, 7, 8, 12) + dc(5, 10, 13, 14)$. Do max term minimization using K map and write simplified P.O.S expression. **(06 Marks)**

c. Write reduced prime implicant table for the
$f(v, w, x, y, z) = \sum m(1, 9, 10, 11) + dc(0, 3, 14, 25, 27)$. Implement using gates. **(10 Marks)**

Module-2

3 a. Write a note on BCD decoders. **(04 Marks)**

b. Implement 3 to 8 line decoder using two 2 to 4 line decoders. **(06 Marks)**

c. Implement $f(a, b, c) = \sum m(0, 2, 4, 7)$ using suitable decoder and with one NAND gate. **(10 Marks)**

OR

4 a. Write a note on 10 line to BCD encoder. **(04 Marks)**

b. Design 1 bit comparator with cascade inputs and outputs. **(08 Marks)**

c. Realize $p = f(a, b, c, d) = \sum m(0, 1, 2, 4, 5, 7, 8, 9, 12, 13)$ using suitably MUX. **(08 Marks)**

Module-3

5 a. Implement 8 bit Adder/subtractor using 7483. **(05 Marks)**

b. Implement 4 to 16 line decoder using two 3 to 8 decoder. **(06 Marks)**

c. Explain how fast carry technique reduces propagation times through parallelAdder. **(09 Marks)**

OR

6 a. Write a note on D flip flop with neat figure and function table, character equation, FF excitation table and applications. **(05 Marks)**

b. Write a note on JK master slave flip flop. **(06 Marks)**

c. Design a counter which has following states and repeats.
0-4-5-2
Use only JK flipflops. **(09 Marks)**

Module-4

7 a. Design a mod 8 synchronous up counter using JK flip flops. **(05 Marks)**

b. Write state diagram for give state table

Pr	Next xy/z							
	00	Z	01	Z	11	Z	10	Z
A	B	0	C	0	B	1	A	0
B	E	0	C	0	B	1	D	1
C	A	0	B	0	C	1	D	1
D	C	0	D	0	A	1	B	0
E	C	0	C	0	C	1	E	0

Table Q.7(b)

(06 Marks)

c. Design a synchronous mod-5 down counter. **(09 Marks)**

OR

8 a. Write a note on universal shift register. **(07 Marks)**

b. Write a note on Mod 8 twisted ring counter with logic diagram, state table, state diagram and timing diagram for positive edge triggered register. **(08 Marks)**

c. The I/P signal shown below are applied to SR latch when initially in it's 0 state. Sketch Q and $\overline{Q}$ o/p signal assuming all timing constraints are satisfied. **(05 Marks)**

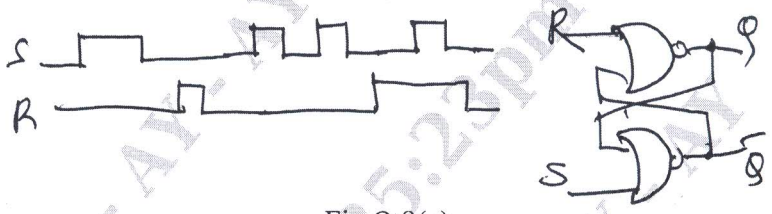

Fig.Q.8(c)

Module-5

9 a. Write a note on Moore machine sequential circuit model with neat diagram. **(05 Marks)**

b. Implement sequential machine for state table 9 (b) using DFF

Present		Next state xy/z											
F_A	F_B	F_A^+	F_B^+	Z	F_A^+	F_B^+	Z	F_A^+	F_B^+	Z	F_A^+	F_B^+	Z
0	0	0	0	0	0	0	0	0	1	0	0	1	0
0	1	0	1	0	1	1	0	1	1	0	0	1	0
1	1	0	0	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	0	0	0	1	1	0	0

Table 9(b)

(07 Marks)

c. Write state table, state diagram, logic diagram and timing diagram for mod 16 up counter using positive edge triggered JK flip flop. **(08 Marks)**

OR

10 a. Write a note on Melay machine sequential circuit model. **(05 Marks)**

b. Implement 3 bit ring counter using 7495 in right shift mode. **(05 Marks)**

c. Write a note on set up time, hold time and delay time relevant to flip flops with waveforms. **(10 Marks)**

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