CBCS SCHEME

USN | | | | | | | | | | |

15EC33

Third Semester B.E. Degree Examination, Feb./Mar. 2022
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define the following terms :
   i) Canonical forms
   ii) Truth Table
   iii) Prime Implicant
   iv) Max term. **(08 Marks)**

b. Simplify the function using K-Map $f(w, x, y, z) = wx + \bar{y}z + w\bar{x}\,\bar{y} + \bar{w} \times yz$. **(08 Marks)**

OR

2 a. Simplify using K-Map and implement it using NAND only.
$f(w, x, y, z) = \Sigma m(2, 6, 7, 8, 9, 10, 12, 13) + dc\,(0, 1, 4)$ **(08 Marks)**

b. Simplify using QM method the function
$f(a, b, c, d) = \Sigma m(1, 3, 6, 8, 9, 10, 12, 14) + dc\,(7, 13)$ **(08 Marks)**

Module-2

3 a. Design 3:8 NAND decoder with active low enable and realize full adder using it. **(08 Marks)**

b. Design 2-bit comparator with necessary truth and K-Map. **(08 Marks)**

OR

4 a. Implement the Boolean function using MUX
   i) 8:1 MUX a, b, c as select lines
   ii) 4:1 MUX with c, d as select lines
$f(a, b, c, d) = \Sigma m(1, 2, 6, 7, 9, 11, 12, 14, 15)$ **(08 Marks)**

b. With a note diagram explain carry lookhead adder. **(08 Marks)**

Module-3

5 a. Explain M/s JK flip-flop (master/slave with neat diagram, truth table and timing diagram. **(08 Marks)**

b. Derive the characteristics equation of JK flip-flop and T flip-flop. **(08 Marks)**

OR

6 a. Explain the following terms :
   i) Latch
   ii) Pulse – Triggered
   iii) Edge –Triggered
   iv) Characteristics equation of D-Flip-flop. **(08 Marks)**

b. Differentiate between :
   i) Sequential Logic circuit and combinational logic circuit
   ii) Flip Flop and Latch. **(08 Marks)**

Module-4

7 a. Explain with a neat diagram universal shift Register along with control modes. **(08 Marks)**

b. Design MOD – 8 asynchronous counter using T-flip-flop. **(08 Marks)**

OR

8 a. Design 3-bit synchronous down counter using T-flip-flop. **(08 Marks)**

b. Design the synchronous counter using D-flip-flop to count the sequence 2 – 4 – 1 – 5 – 0. **(08 Marks)**

Module-5

9 a. Explain Mealy machine model and Moore machine model. **(08 Marks)**

b. Design a synchronous counter using T flip-flops to count the sequence 6 – 5 – 4 – 3 – 2 – 1. **(08 Marks)**

OR

10 a. Analyse the synchronous circuit as in Fig Q10(a).

i) Derive the excitation and output equations
ii) Write the state equations
iii) Construct transition table and state table
iv) Draw the state diagram

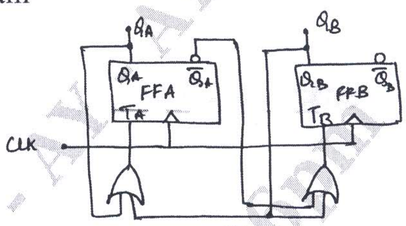

Fig Q10(a) **(08 Marks)**

b. Define the following terms :

i) State table
ii) Transition table
iii) Excitation table
iv) State Diagram. **(08 Marks)**

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