CBCS SCHEME

Third Semester B.E. Degree Examination, July/August 2021
Digital System Design

Time: 3 hrs.   Max. Marks:100

Note: *Answer any FIVE full questions.*

1   a.   Which is the code used for naming the k-map and why?   **(03 Marks)**
     b.   Assuming that the inputs ABCD = 1001, 1010, 1011 and 1101 never occur, determine a simplified expression using k-map.
        $F = \overline{AB}\overline{CD} + \overline{AB}D + \overline{A}CD + ABD + ABC$.   **(07 Marks)**
     c.   Simplify using Quine – McCluskey's technique
        $f(ABCD) = \sum m(6,7,9,10,13) + \sum d(1,4,5,11,15)$.   **(10 Marks)**

2   a.   What are don't cares? Explain with an example.   **(03 Marks)**
     b.   Convert the following Boolean expression into max-term canonical formula and minimize using k-map. $P = X + XY(Y + Z)$.   **(07 Marks)**
     c.   Simplify using k-map :
        $F(v, w, x, y, z) = \sum m(0, 2, 7, 8, 10, 15, 16, 18, 22, 24, 26, 30) + \sum d(6, 12, 14, 23, 31)$.   **(10 Marks)**

3   a.   What is the necessity of carry look-ahead circuit? How will its use enhance the operation of a 4-bit parallel adder?   **(10 Marks)**
     b.   Design and implement a single-bit comparator with G, E and L as outputs using a single 2 – 4 decoder.   **(04 Marks)**
     c.   Implement the following Boolean function using a 8 : 1 MUX with a, b and d as select inputs $f(a, b, c, d) = \sum m(4,5,7,8,10,12,15)$.   **(06 Marks)**

4   a.   Implement a full subtractor using 2 – 4 decoder.   **(06 Marks)**
     b.   Implement the following Boolean expression using 8 : 1 MUX with A, C and D as select inputs $F = \overline{BD} + A\overline{B}C + \overline{C}D + \overline{AB}\overline{C}D$.   **(08 Marks)**
     c.   What is a BCD to 7 – segment decoder? Explain the operation with the function table.   **(06 Marks)**

5   a.   Explain the application of SR latch as a switch debouncer with waveforms.   **(06 Marks)**
     b.   What is race around condition? Explain its elimination in MSJKFF through its working and timing diagram.   **(10 Marks)**
     c.   Obtain the characteristic equation of a JKFF.   **(04 Marks)**

6   a.   What is the necessity of converting SRFF into a JKFF? Explain the operating of a JKFF with timing diagram.   **(07 Marks)**
     b.   Justify the operation of an edge triggered D-FF with a timing diagram. Also explain as to how transition occurs only on an edge and not during a level of clock signal.   **(10 Marks)**
     c.   What is triggering? What are the different methods of triggering?   **(03 Marks)**

7   a.   Write the circuit diagram of a 4-bit shift register with 4 DFFs and 4 2 : 1 MUX. Explain its operation in different modes.   **(10 Marks)**
     b.   Design a synchronous counter for the counting sequence 3, 2, 5, 1, 0, 3 - - - using JKFF.   **(10 Marks)**

8 a. With a neat diagram and mode table, explain the operation of a 4-bit universal shift register.
       (10 Marks)
   b. Design an asynchronous mod-5 up counter using TFF with counting sequence :
       7, 8, 9, 10, 11, 7- - - . **(06 Marks)**
   c. Explain the operation of a 4-bit ring counter using shift register. **(04 Marks)**

9 a. Give a comparison between a Mealy and Moore model of synchronous sequential circuit
       through block diagram. **(06 Marks)**
   b. Bring out a comparison between RAM and ROM memories. **(04 Marks)**
   c. Analyse a synchronous sequential circuit by determing excitation equations, excitation table,
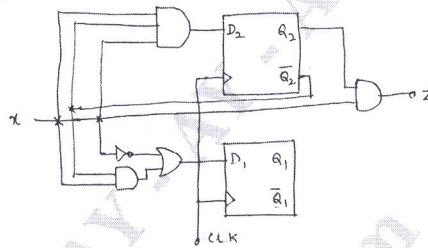   state table and state diagram.

Fig.Q9(a) **(10 Marks)**

10 a. Compare combinational and sequential circuits. **(02 Marks)**
   b. Give the structure and operation of flash memory. How is it different from EEPROM?
       (08 Marks)
   c. Design a synchronous sequential circuit for the given state diagram. Also obtain transition
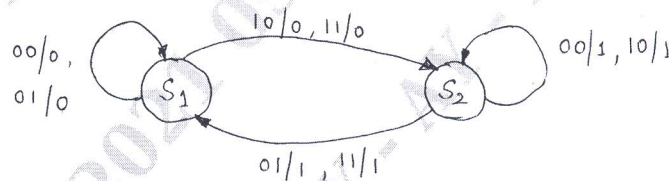   table, state table and excitation table.

Fig.Q10(c)

Assume S_1 and S_2 as '0' and '1' respectively and use T-FF. **(10 Marks)**

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