CBCS SCHEME

USN | | | | | | | | | |

17MT36

Third Semester B.E. Degree Examination, July/August 2021
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions.

1 a. Explain the basic operational concept between processor and memory (connection between memory and processor) **(10 Marks)**

b. Explain branching concept by considering example of adding "N" number using straight line program and using loop. **(10 Marks)**

2 a. Explain BIG ENDIAN and LITTLE ENDIAN methods with example. **(10 Marks)**

b. Explain with a neat time line diagram, how the user program and OS routine share the processor for reading a machine level language data and print the results. **(10 Marks)**

3 a. What are addressing modes? Explain the (i) Direct (ii) Indirect (iii) Register (iv) Immediate (v) Relative addressing mode. **(10 Marks)**

b. Explain the logical shift, arithmetic shift and rotate instructions with examples. **(10 Marks)**

4 a. What is stack? Explain the operation of push and pop with instructions. **(10 Marks)**

b. What are assembler directives? Explain assembler directives with example program. **(10 Marks)**

5 a. Explain Direct Memory Access in detail. **(10 Marks)**

b. Explain the steps involved in enabling and disabling of interrupts. **(10 Marks)**

6 a. What are interrupts? Explain transfer of control through the use of interrupts. **(10 Marks)**

b. Explain the steps involved in handling the interrupt from multiple devices. **(10 Marks)**

7 a. Draw and explain the organization of the 2M × 8 dynamic memory chip. **(10 Marks)**

b. Explain the operation of a synchronous DRAM along with a burst read of length 4 in a SDRAM. **(10 Marks)**

8 a. Define the cache, write through protocol, write back protocol and load through protocol. **(10 Marks)**

b. Define, what is virtual memory and explain with a neat diagram. **(10 Marks)**

9 a. Explain the single bus organization of the data path inside a processor with a neat diagram. **(10 Marks)**

b. Explain and write the control sequences for execution of the instruction Add (R_3), R_1. **(10 Marks)**

10 a. Explain multi-bus organization of the data path with a neat diagram. **(10 Marks)**

b. Write the control sequence for conditional and unconditional branch instruction. **(10 Marks)**

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