15MT35

(06 Marks)

Third Semester B.E. Degree Examination, July/August 2021 Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions.

a.	With a neat circuit diagram analyze the operation of full wave rectifier with a C filter and
	also evaluate the expression for ripple factor. (10 Marks)
b.	Explain the following terms with respect to PN junction model:
	i) Reverse recovery time
	ii) Transition capacitance. (06 Marks)
a.	Draw the VI characteristics of a semiconductor diode and explain it. (08 Marks)
b.	Construct a double ended clipper circuit to clip the output waveform at +2V and -3V from
	10V (p-p) supply voltage. (08 Marks)
a.	With a neat sketch, explain the operation of first order low pass Butterworth filter. Also
	derive the expression for gain. (10 Marks)
	b. a. b.

4	a.	With a neat sketch, explain the operation of notch filter. Design a wide band pass filter with $f_L = 200$ Hz and $f_H = 1$ kHz, pass band gain =	(08 Marks) 4 calculate
		the value of quality factor.	(08 Marks)

b. Design a RC phase shift oscillator with frequency $f_0 = 200 Hz$.

5	a.	Explain the working of astable	multivibrator with	n a neat circuit,	necessary	waveform and
		relevant expressions.				(10 Marks)
	b.	Design a divide by 2 network	using monostable	multivibrator for	r the inpu	t trigger signal

Design a divide by 2 network using monostable multivibrator for the input trigger signal 2kHz with value of $e = 0.01 \mu F$. (06 Marks)

6	a.	With a neat s	ketch, e	xplain the op	eratio	n Schmi	tt trigger circu	ıt.				1	Marks)
	b.	With a neat	sketch	demonstrate	how	astable	multivibrator	can	be	used	as	square	wave
		generator.											Marks)

7	a. With a neat sketch, explain TTL logic.	(10 Marks)
	b. Implement NAND and NOR gate using CMOS logic.	(06 Marks)

8	a.	Implement the following using universal gates (NAND and NOR):	
		i) NOT ii) AND iii) OR iv) EX-OR.	(10 Marks)
	b.	With a neat circuit implement 3 bit synchronous upcounter.	(06 Marks)

9	a.	Define multiplexer. Implement a 4 × 1 MUX using logic gates.	(08 Marks)
		Explain the operation of successive approximation ADC.	(08 Marks)

10	a.	Design a 3×8 decoder using 2×4 decoder.	(08 Marks)
	b.	Explain the operation of R-2R DAC with neat sketch.	(08 Marks)

* * * *

Important Note: 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.

2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.