CBCS SCHEME

USN | | | | | | | | | | |

15MT36

Third Semester B.E. Degree Examination, July/August 2021
Computer Organization

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions.***

1 a. Explain the basic operational concepts between the processor and memory. **(08 Marks)**

b. How to measure the performance of the computer using performance equation? **(08 Marks)**

2 a. Explain the following instruction with example :
i) MOVE LOC, R1 ii) ADD A, B, C iii) STORE R_i, A
iv) LOAD A, R_6 v) SUBTRACT$(R1)_1$+ R5 **(10 Marks)**

b. Explain BIG-ENDIAN and LITTLE – ENDIAN methods with example. **(06 Marks)**

3 a. Define an addressing mode. Explain the following addressing modes with example:
i) Immediate
ii) Indirect
iii) Index
iv) Relative
v) Auto increment and auto decrement. **(10 Marks)**

b. There are n = 100 numbers stored in the memory location starting from NUM 1 at 208. Each of the numbers is word organized. It is required to add these numbers and store at memory location SUM. Write an assembly language program to perform this task. Use the necessary assembler directives. **(06 Marks)**

4 a. Registers R5 is used in a program to point to the top of a stack. Write a sequence of instruction using the index, auto increment and auto decrement addressing modes to perform each of the following tasks:
i) POP the top two items off the stack, add them and then push the result onto the stack.
ii) COPY the fifth item from the top into register R_8.
iii) Remove the top ten items from the stack. **(04 Marks)**

b. Both of the following statements cause the value 300 to be stored in location 1000, but at different times.

```
ORIGIN 1000
DATAWORD 300
```

and

```
MOVE # 300, 1000
```

(04 Marks)

c. What is subroutine linkage? With example explain different ways of passing parameters to subroutines. **(08 Marks)**

5 a. Explain any two methods of handling multiple devices using interrupt priority schemes. **(08 Marks)**

b. Draw the timing diagram of input data transfer using multiple clock cycles and explain the operation. **(08 Marks)**

6 a. Draw the diagram of DMA controller interface in a computer system and explain the working principle. (08 Marks)
b. Draw the timing diagram of PCI bus read operation and explain. (08 Marks)

7 a. Analyze the internal organization of a 2M × 8 (16M) DRAM chip. (08 Marks)
b. Explain the working of a CMOS memory cell. (08 Marks)

8 a. What is a cache? Explain any two cache mapping functions with neat sketches. (10 Marks)
b. Define :
i) memory latency
ii) hit – rate
iii) miss penalty. (06 Marks)

9 a. Write the single bus organization of the data paths inside a processor and explain the importance of each unit. (10 Marks)
b. Write and explain the control sequence for execution of an unconditional branch instruction. (06 Marks)

10 a. Draw and explain multiple bus organization. (08 Marks)
b. With a neat block diagram, explain hardwired control unit show the generation Zin and End control signal. (08 Marks)

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