CBCS SCHEME

17EC53

Fifth Semester B.E. Degree Examination, July/August 2021
Verilog HDL

Time: 3 hrs.   Max. Marks: 100

Note: *Answer any FIVE full questions.*

1   a.   Explain the typical design flow for designing VLSI IC circuits.   **(10 Marks)**
    b.   Discuss the evaluation of computer aided design.   **(05 Marks)**
    c.   Explain top-down design methodology.   **(05 Marks)**

2   a.   Discuss modules, instances with the help of 4-bit ripple carry counter example.   **(10 Marks)**
    b.   Describe instance and instantiation with example.   **(05 Marks)**
    c.   Explain stimulus and design block with an example.   **(05 Marks)**

3   a.   Discuss the data types used in verilog with an example.   **(10 Marks)**
    b.   Explain system task and compiler directives in verilog.   **(10 Marks)**

4   a.   Explain components of verilog module with an example.   **(10 Marks)**
    b.   Explain port declaration, port connection rules and connecting ports to external signals.
                                                                                           (10 Marks)

5   a.   Write a verilog gate level description for 4:1 multiplexes also write stimulus block.
                                                                                           (10 Marks)
    b.   Explain rise delay, fall delay, turn off delay, min value, typical value and max value.
                                                                                           (10 Marks)

6   a.   Describe continuous assignment statement and implicit continuous assignment statement.
                                                                                           (10 Marks)
    b.   Explain arithmetic and logical operators with example.   **(10 Marks)**

7   a.   Explain blocking and non blocking procedural assignment in behavioral modeling. **(10 Marks)**
    b.   Describe event-based-timing control mechanism in behavioral modeling.   **(10 Marks)**

8   a.   Explain conditional statements. Using if and else write a verilog HDL program for D_FF.
                                                                                           (10 Marks)
    b.   Describe multiway branching. Use case statement and write verilog program for 3-bit binary
         counter.   **(10 Marks)**

9   a.   Why we use VHDL? What are the short comings of VHDL?   **(10 Marks)**
    b.   Describe the design in VHDL.   **(10 Marks)**

10 a.   Discuss the basic building block of VHDL design with an example of dataflow/behavioral
         description.   **(10 Marks)**
    b.   Write a VHDL description for 4 bit ripple carry adder, also write the circuit diagram for
         same.   **(10 Marks)**

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