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10EC56

Fifth Semester B.E. Degree Examination, July/August 2021
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain the Fabrication steps of CMOS-P-Well process with neat diagram, write the mask sequence. **(10 Marks)**

b. Explain second order effects with respect to a MOS device. **(10 Marks)**

2 a. With neat circuit diagram and relevant mathematical equations explain differential inverter. **(10 Marks)**

b. Draw the circuit schematic, stick diagram and layout diagram of nMOS, 2 I/P Nand Gate. **(10 Marks)**

3 a. Describe the following logic structures:
i) Complementary CMOS logic
ii) Pseudo nMOS logic. **(10 Marks)**

b. Explain the operation of CMOS dynamic logic. Also discuss the cascading problems of dynamic CMOS logic. **(10 Marks)**

4 a. Calculate the capacitance of the structure given below.

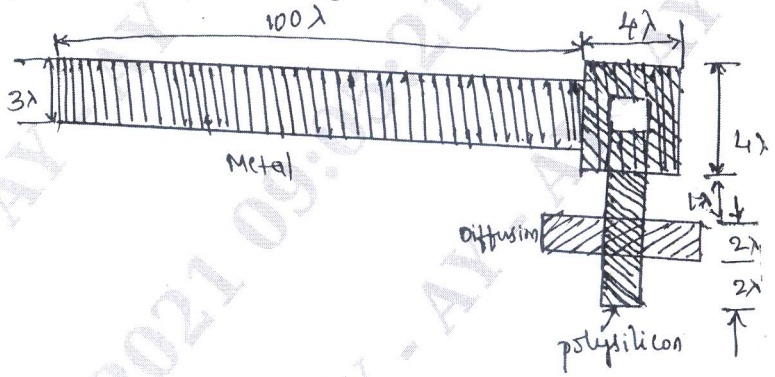

Fig.Q.4(a)

Relative area capacitance values
Metal 1 to substrate = 0.075
Polysilicon to substrate = 0.1
Gate to channel = 1.0 **(10 Marks)**

b. Obtain the scaling factors for the following device parameters.
i) Gate capacitance per unit area (C_o)
ii) Channel resistance (R_{on})
iii) Gate Delay (T_D)
iv) Saturation current (I_{dss})
v) Power dissipation / Gate P_g. **(10 Marks)**

5 a. Discuss the architectural issues related to subsystem design. (10 Marks)
b. Explain dynamic register element and 4 bit shift register using nMOS and CMOS logic. (10 Marks)

6 a. Design 4×4 barrel shifter. (10 Marks)
b. With the neat diagram, explain parity generator structured design. (10 Marks)

7 a. Explain three transistor dynamic RAM cell. (10 Marks)
b. Explain CMOS pseudo static memory cell. (10 Marks)

8 a. Explain scan design techniques. (10 Marks)
b. Write short notes on:
i) Noise Margin
ii) I/O pads
iii) Silicides. (10 Marks)

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