CBCS SCHEME
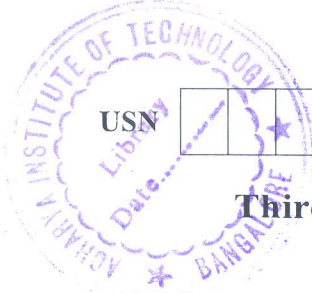
17EC34

Third Semester B.E. Degree Examination, July/August 2021
Digital Electronics

Time: 3 hrs.   Max. Marks: 100

Note: *Answer any FIVE full questions.*

1   a. Define the following with an example: (i) Sum of products (ii) Product of sums (iii) Canonical sum of products (iv) Canonical product of sums (v) Minterm. **(10 Marks)**
    b. Obtain the minimal logical expression for the given minterm using K-map.
        $T = f(a,b,c,d,e) = \sum(0,2,8,10,16,18,24,26)$ **(05 Marks)**
    c. Simplify the following maxterm expression using K-map:
        $A = f(w, x, y, z) = \pi(2, 3, 8, 9, 10, 11, 12, 13, 14, 15)$ **(05 Marks)**

2   a. Simplify the following using Quine-McClusky minimization technique and also verify the same.
        $D = f(a,b,c,d) = \sum(0,1,2,3,6,7,8,9,14,15)$ **(10 Marks)**
    b. Express the following SOP equations in the form of minterms:
        (i) $G = f(A,B,C) = A'BC + A'B'C + ABC$
        (ii) $P = f(w, x, y, z) = wxyz' + wx'yz' + w'xyz' + w'x'yz'$ **(04 Marks)**
    c. Place the following equations into proper canonical form:
        (i) $P = f(a,b,c) = ab' + ac' + bc$
        (ii) $T = f(a,b,c) = (a + b')(b' + c)$ **(06 Marks)**

3   a. Define : (i) Subtractors   (ii) Binary comparators   (iii) Full Adder **(06 Marks)**
    b. Realize the following using 745151 8 : 1 MUX :
        (i) $F = f(x, y, z) = \sum(1,2,4,5,7)$
        (ii) $T = f(w, x, y, z) = \sum(0,1,2,4,5,7,8,9,12,13)$ **(06 Marks)**
    c. Write the truth table of two-bit magnitude comparator. Write the K-map for each. Output of two-bit magnitude comparator and the resulting equation. **(08 Marks)**

4   a. Design a 4-to-16 Decoder using two 74XX138 decoders. **(05 Marks)**
    b. With a neat diagram, explain carry look ahead adder. **(10 Marks)**
    c. Distinguish between decoder and encoder. Implement full adder using IC74153. **(05 Marks)**

5   a. Explain Master Slave JK flip-flop with the help of timing diagram and waveforms. **(08 Marks)**
    b. Find the characteristic equation of T and SR flip-flops with the help of functional tables. **(06 Marks)**
    c. With a neat diagram, explain positive edge triggered D-flip flop and explain for different input conditions. **(06 Marks)**

6 a. Explain the operation of switch debouncer built using SR latch with the help of waveforms.

(04 Marks)

b. What is a flip-flop? Discuss the working principle of Master Slave SR f/f with the help of timing diagram and truth table. (08 Marks)

c. Define : (i) Propagation delay   (ii) Minimum pulse width   (iii) Setup time and
(iv) Hold time (08 Marks)

7 a. Design a mod-6 synchronous counter using clocked D flip flop. (08 Marks)

b. Explain SIPO and SISO using flip flop. (06 Marks)

c. Design synchronous mod-6 counter using clocked JK flip flops. (06 Marks)

8 a. Explain mod-8 and mod-7 twisted ring counter with a neat diagram and counting sequence.

(08 Marks)

b. Explain 4-bit binary ripple counter with logic diagram, timing diagram and counting sequence. (08 Marks)

c. Explain mod-4 ring counter with logic diagram and counting sequence. (04 Marks)

9 a. Explain Kealy and Moore sequential circuit model with neat diagrams. (06 Marks)

b. Define : (i) Input variable   (ii) Output variable   (iii) State variable and (iv) State.

(04 Marks)

c. Give Mealy state notation, Moore circuit notation and Mealy and Moore mixed circuit diagram notation for JK flip flop. (10 Marks)

10 a. Give the steps for analyzing the function of a sequential circuit. (04 Marks)

b. Explain JK flip flop characteristic table excitation table with K-maps for excitation variables. (10 Marks)

c. Explain the excitation realization for T and D-flip-flops. (06 Marks)

* * * * *