CBCS SCHEME

USN | | | | | | | | | | |

15EC33

Third Semester B.E. Degree Examination, July/August 2021
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions.***

1 a. Convert the given Boolean function into
   i) $Y = f(a, b, c) = (a + b)(b + c)$ minterm canonical form.
   ii) $P = f(a, b, c) = a + ac(b + c)$ maxterm canonical form. **(08 Marks)**

b. Determine the prime implicants and essential prime implicants and also simplify the given boolean function using K-map method.
$N = f(a, b, c, d) = \pi M(0, 1, 4, 5, 8, 9, 11) + dc(2, 10)$. **(08 Marks)**

2 a. Simplify the given function in POS form using K-map method and implement using NOR gates. $P = f(a, b, c, d) = \pi M(1,3, 8, 10, 12, 13, 14, 15)$. **(08 Marks)**

b. Simplify using QM minimization technique.
$V = f(a, b, c, d) = \pi m(1, 5, 7, 9, 13, 15) + \Sigma d(8, 10, 11, 14)$ **(08 Marks)**

3 a. Explain carry look ahead adder with neat diagram and relevant expressions. **(08 Marks)**

b. Implement the following multiple output functions using 3:8 decoders (IC-74138).
   i) $f_1(a, b, c, d) = \pi M(2, 4, 5, 7, 9, 10, 13, 14)$
   ii) $f_2(a, b, c, d) = \Sigma m(1, 3, 5, 8, 12, 14, 15)$. **(08 Marks)**

4 a. Design 2-bit comparator and briefly explain. **(08 Marks)**

b. Implement $f(a, b, c, d) = \Sigma m(0, 1, 5, 6, 10, 12, 14, 15)$
Using : i) 8:1 MUX with a, b, c as select lines
   ii) 4:1 MUX with c, d as select lines. **(08 Marks)**

5 a. Design SR latch and also apply it in switch debouncer circuit, explain the operations using suitable waveforms. **(08 Marks)**

b. Explain the working of Master-Slave JK flip-flop with the help of logic diagram, function table, logic symbol and timing diagram. **(08 Marks)**

6 a. With a neat logic diagram, explain the working of positive edge triggered D-flip-flop, also draw the timing diagram. **(08 Marks)**

b. Obtain the characteristics equations of JK flip-flop, SR flip-flop and T flip-flop. **(08 Marks)**

7 a. Describe the working principle of universal shift register with the help of logic diagram and mode control table. **(08 Marks)**

b. Illustrate the operation of 4-bit binary ripple counter using logic diagram and timing diagram. **(08 Marks)**

8 a. Explain the working of 4-bit Johnson counter using positive edge triggered D flip-flop, also draw the timing diagram. What is the modulus of this counter? **(08 Marks)**

b. Design a Mod-6 synchronous counter using JK flip-flop. **(08 Marks)**

9 a. Explain Mealy and Moore model of clocked synchronous sequential circuit with the block diagram. **(08 Marks)**

b. Design a cyclic mod – 8 synchronous binary counter using JK flip – flop. Give state diagram, transition table and excitation table. **(08 Marks)**

10 a. Construct a Mealy state diagram that will detect input sequence 10110, when input pattern is detected Z is asserted high. Write the state diagram. **(08 Marks)**

b. Analyze the following sequential circuit shown in Fig Q10(b) and obtain

i) Flip – Flop input and output equation
ii) Transition equation (ch.equ)
iii) Transition table
iv) State table
v) Draw state diagram.

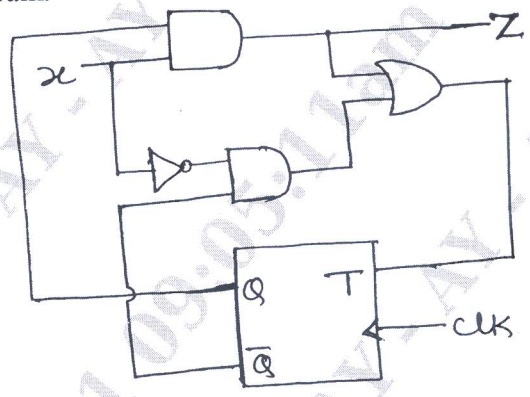

Fig Q10(b) **(08 Marks)**

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