CBCS SCHEME

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17CS72

Seventh Semester B.E. Degree Examination, July/August 2021
Advanced Computer Architecture

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions.***

1 a. List the performance factors and system attributes. Explain how performance factors are influenced by system attributes. **(08 Marks)**

b. What are the conditions of parallelism? Explain the types of data dependence. **(06 Marks)**

c. With a neat diagram, explain the levels of parallelism in program execution on modern computers. **(06 Marks)**

2 a. Consider the execution of an object code with 2×106 instructions on a 400 MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment.

Instruction type	CPI	Instruction mix
Arithmetic and Logic	1	60%
Load/store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

i) Calculate the average CPI when the program is executed on a uniprocessor with the above trace results.

ii) Calculate the corresponding MIPS rate based on the CPI obtained. **(07 Marks)**

b. Explain the architecture of vector super computer with a neat diagram. **(07 Marks)**

c. Discuss in detail : i) UMA model ii) NUMA model iii) COMA model. **(06 Marks)**

3 a. Explain the architecture of VLIW processor and its pipeline operations. **(08 Marks)**

b. Distinguish between typical RISC and CISC processor architectures. **(06 Marks)**

c. With a neat diagram, explain the hierarchical memory technology. **(06 Marks)**

4 a. Explain Inclusion, Coherence and Locality properties. **(06 Marks)**

b. Briefly explain the virtual memory models for multiprocessor system. **(06 Marks)**

c. With a diagram, explain a typical superscalar RISC processor architecture consisting of an integer unit and a floating point unit. **(08 Marks)**

5 a. Explain bus arbitration and its types in multiprocessor systems. **(08 Marks)**

b. Explain Prefetch buffer and Internal data forwarding mechanism used in instruction pipelining. **(06 Marks)**

c. Explain Sequential and Weak consistency models. **(06 Marks)**

6 a. Explain with diagram, the Backplane bus specification. **(06 Marks)**

b. Explain multiply pipeline design to multiply two 8 bit integers
X = 10110101 , Y = 10010011. **(06 Marks)**

c. For the reservation table of a non linear pipeline shown below :

	0	1	2	3	4
S_1	X				X
S_2			X		
S_3				X	

i) What are the forbidden latencies? Write initial collision vector.
ii) Draw the state transition diagram.
iii) List all simple cycles and greedy cycles.
iv) Determine MAL. **(08 Marks)**

7 a. Explain briefly different vector access memory schemes. **(06 Marks)**
b. Explain four context switching policies. **(08 Marks)**
c. Explain routing in Omega network. **(06 Marks)**

8 a. Explain Snoopy protocols, with its approaches. **(10 Marks)**
b. With a diagram, explain the architecture of the connection machine CM - 2. **(10 Marks)**

9 a. Explain the fairness policies and sole access protocols in the principles of synchronization. **(07 Marks)**
b. What are the major hurdles of pipelining? Illustrate the branch hazards in detail. **(07 Marks)**
c. Define Parallel programming model. Explain any 2 models. **(06 Marks)**

10 a. What are the issues in using shared variable model? **(07 Marks)**
b. With the help of a neat diagram, explain compilation phases in code generator. **(07 Marks)**
c. Explain different language features for parallelism. **(06 Marks)**

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