CBCS SCHEME

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15CS72

Seventh Semester B.E. Degree Examination, July/August 2021
Advanced Computer Architectures

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions.***

1 a. Explain the vector super computer with neat diagram. **(06 Marks)**

b. Trace out the following program to detect parallelism using Bernstein's condition

P1 : C = D × E
P2 : M = G + C
P3 : A = B + C
P4 : C = L + M
P5 : F = G ÷ F

Assume that each steps requires steps to execute and 2 address are available. Compare between sequential and parallel execution of the above program. **(06 Marks)**

c. Explain the factor which affects the performance of network. **(04 Marks)**

2 a. Explain how grain packing can be done to compute the sum of 4 elements in the resulting product matrix C = A × B what matrices A and B are order 2 × 2. **(10 Marks)**

b. Consider the execution of an direct code with 2×10^6 instructions on a 40MHz processor. The the program consists of 4 major types of instructions. The instruction mix and the number and cycle (CPI) needed for each instruction type are given below based on the result of program trace experiment.

Instruction type	CPI	Instruction mix
Arithmetic and logic	1	60%
Load/store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

i) Find total number of cycle required to execute the program
ii) Calculate the average CPI after the program is executed in uniprocessors
iii) Calculate MIPS Rate. **(06 Marks)**

3 a. Explain super scalar RISC processor architecture consisting of an integer unit and floating point unit with diagram. **(08 Marks)**

b. With diagram, explain memory hierarchy technology. **(08 Marks)**

4 a. Discuss and compare the characteristics of CISC and RISC Architectures. **(08 Marks)**

b. Explain with neat diagram and a Very Long Instruction Word (VLIW) processor and its pipeline operations. **(08 Marks)**

5 a. Explain set associative cache organization and discuss on its design trade off. **(08 Marks)**

b. With respect to shared memory organization, explain the memory interleaving techniques. **(08 Marks)**

6 a. Design a binary integer multiply pipe line with five stages. The first stage is for partial product generation. The last stage is a 36-bit carry look ahead Adder. The middle three stages are made 16 Carry Save Address (CSAs) of appropriate lengths

i) Prepare a schematic design of the five stage multiply pipeline. All line width and interchange connections must be shown

ii) Determine the maximal clock rate of the pipeline if the stage delays are $t_1 = t_2 = t_3 = t_4 = 90ns$ $t_5 = 45ns$ and the latch delay is 20ns.

iii) What is the maximal through put of this pipeline in terms of the number of 36-bit results generated per second? **(08 Marks)**

b. Explain Asynchronous mode and clocking in linear pipeline processor. **(08 Marks)**

7 a. What is cache coherence problem? Explain Goodman's write once cache coherence protocol. **(08 Marks)**

b. With appropriate figure, derive a formula to find communication latency in store and forward and wormhole routing method. **(04 Marks)**

c. Explain virtual channel versus physical channel associated with message passing mechanism. **(04 Marks)**

8 a. Explain the sharing list creation and update method used in the IEEE scalable coherence interface standard. **(08 Marks)**

b. Explain the effects of using relaxed consistency memory model in scalable multiprocessor with multithreading. **(08 Marks)**

9 a. Explain the dynamic instruction scheduling using Tomasulo's algorithm. **(08 Marks)**

b. Explain with neat diagram and the major phases of parallelizing compiler. **(08 Marks)**

10 a. Explain any three methods for implementing efficient synchronization schema. **(08 Marks)**

b. Write note on :

i) Reorder buffer

ii) Register renaming. **(08 Marks)**

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