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18CS33

Third Semester B.E. Degree Examination, July/August 2021 Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions.

- 1 a. With a neat sketch, explain the construction and working of Light Emitting Diode (LED). (06 Marks)
- b. For the given circuit in Fig.Q.1(b) Si transistor with $\beta = 50$, calculate the I_B , I_C and V_{CE} . Draw the DC load line and determine the operating point. (06 Marks)

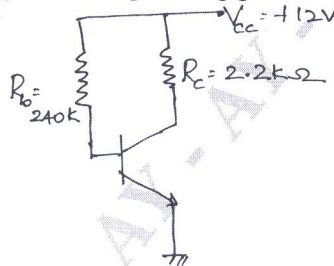


Fig.Q.1(b)

- c. With a neat circuit diagram and waveform, explain the working of Astable multivibrator. (08 Marks)
- 2 a. What is a filter? Compare between active filters and passive filters. (06 Marks)
- b. With a neat diagram and waveform, explain working of relaxation oscillator. (08 Marks)
- c. Explain the different components of regulated power supply. (06 Marks)
- 3 a. Simply the given expression using K-map $F(A, B, C, D) = \sum m(0, 1, 4, 8, 9, 10) + \sum d(2, 11)$ (08 Marks)
- b. Using a prime-implicant charts, find all minimum SOP solution using Quine-Mc-Clusky method for $f(w, x, y, z) = \sum m(1, 3, 4, 5, 6, 7, 10, 12, 13) + \sum d(2, 9, 15)$. (12 Marks)
- 4 a. Find all prime implicants of the following given function and find all minimum solutions using Petrick method. $F(A, B, C, D) = \sum m(7, 12, 14, 15) + \sum d(1, 3, 5, 8, 10, 11, 13)$ (12 Marks)
- b. Using the map-entered variable, use 4 variable maps to find the minimum SOP expression for the function $G(A, B, C, D, E, F) = m_0 + m_2 + m_3 + Em_5 + Em_7 + Em_9 + m_{11} + m_{15} + d(1, 10, 13)$ (08 Marks)
- 5 a. Write the truth table for the AND-OR functions for four valued simulations. (06 Marks)
- b. With a suitable assumption, explain the timing diagram of an AND-OR circuit. (06 Marks)
- c. What is hazard? Explain the different type of hazard with an example. (08 Marks)
- 6 a. Explain multiplexer with an example. Realize the 8:1 multiplexer using 2:1 and 4:1 multiplexer. (08 Marks)
- b. With a neat diagram, explain the 3 to 8 decoder. (06 Marks)
- c. With a neat sketch, explain the structure of PLA. (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

- 7 a. Explain the structure of an VHDL module. Write a VHDL code for 4:1 multiplexer. (08 Marks)
b. Write a program for the implementation of full-Adder using VHDL. (06 Marks)
c. With a neat diagram, explain switch debouncing circuit using an S-R latch. (06 Marks)
- 8 a. What is a flip flop? Explain the gated D-latch, with a neat diagram. (06 Marks)
b. Explain the Master-Slave J-K flip-flop with a neat diagram, using NAND gates. (10 Marks)
c. Explain T-flip flop with a diagram. (04 Marks)
- 9 a. What is Register? With a neat diagram, explain the register with data, load, clear and clock inputs. (08 Marks)
b. With a neat sketch, explain the working of Serial In Serial Out (SISO) Right shift register. (06 Marks)
c. What are the difference between the synchronous and Asynchronous counters? (06 Marks)
- 10 a. Design a synchronous counter for the sequence $0 \rightarrow 3 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 7 \rightarrow 0 \rightarrow 3$ using J-K flip-flop. (10 Marks)
b. Design a counter using S-R flip-flop for the following given count $0 \rightarrow 4 \rightarrow 7 \rightarrow 2 \rightarrow 3 \rightarrow 0$. (10 Marks)
