

USN

1A414EC048

10EC63/10EC638

Sixth Semester B.E. Degree Examination, Jan./Feb. 2021

### Microelectronics Circuits

Time: 3 hrs.

Max. Marks:100

Note: Answer any FIVE full questions, selecting THREE questions from Part-A and TWO questions from Part-B.

#### PART - A

- 1 a. Explain the implementation of biasing circuit by fixing  $V_G$  and connecting a resistance in the source with neat diagram. (06 Marks)
- b. Design the circuit in Fig.Q1(b) to establish a drain voltage of 0.1V. What is the effective resistance between drain and source at this operating point. Let  $V_t = 1V$ ,  $K'_n \left( \frac{W}{L} \right) = 1 \text{ mA/V}^2$ .

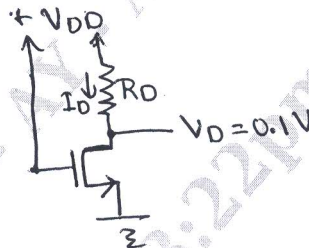


Fig.Q1(b)

- c. Explain common gate amplifier with neat circuit diagram and small signal equivalent circuit. (08 Marks)
- 2 a. Compare MOSFET and BJT in terms of :  
(i) Low frequency hybrid  $\pi$  model  
(ii) Current voltage characteristics  
(iii) High frequency model (06 Marks)
- b. With relevant equations and neat circuit diagram, explain working of MOS steering circuits. (08 Marks)
- c. With neat diagram, explain working of basic MOS current mirror circuit. (06 Marks)
- 3 a. Draw high frequency equivalent circuit model of common source amplifier and analyze using Miller's theorem. (08 Marks)
- b. Analyze common base amplifier to find  $R_{in}$  and  $R_{out}$ . (07 Marks)
- c. How does cascade MOS current mirror improves the performance of current mirror circuit? (05 Marks)
- 4 a. With neat diagrams, explain small signal operation of MOS differential pair. Derive expression for differential gain. (10 Marks)
- b. For circuit in Fig.Q4(b), the differential amplifier uses transistor with  $\beta = 100$ . Evaluate:  
(i) Input differential Resistance  $R_{id}$   
(ii) Overall differential gain  $\frac{V_o}{V_{sig}}$  (neglect effect of  $r_o$ )

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

- (iii) The worst case common mode gain if the 2 collector resistances are accurate to within  $\pm 1\%$ .
- (iv) The CMRR in dB.
- (v) The input common mode resistance (assume  $V_A = 100$  V)

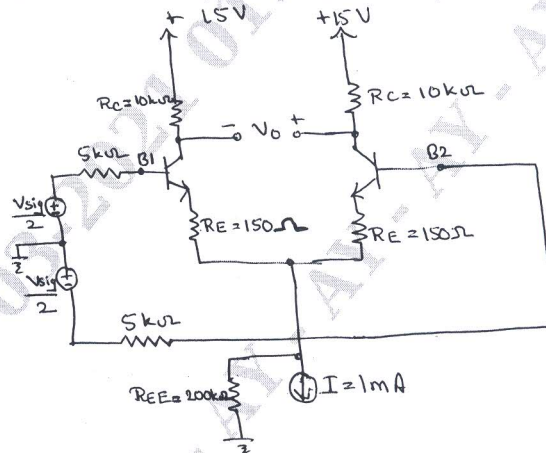


Fig.Q4(b)

(10 Marks)

5 Write short notes on:

- T-equivalent circuit model of MOSFET
- Multistage amplifiers
- Source follower
- Current source

(20 Marks)

### PART - B

- Explain the three properties of negative feedback. (09 Marks)
  - Draw and explain Nyquist plot of an unstable amplifier. (05 Marks)
  - With graph, explain how stability analysis is done using bode plot. (06 Marks)
- With neat diagram, explain a single op amp difference amplifier and derive an expression for differential gain  $A_d$ . (07 Marks)
  - Briefly explain logarithmic amplifier and derive an expression for output voltage. (08 Marks)
  - Explain basic principle of sample and hold circuit using basic circuit. (05 Marks)
- Write a short note on domino CMOS logic circuits. (06 Marks)
  - Implement  $F = AB + \overline{A}B$  using AOI gate logic. (08 Marks)
  - Explain the Voltage Transfer Characteristics (VTC) of CMOS inverter when  $Q_N$  and  $Q_P$  are matched. (06 Marks)

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