

# CBCS SCHEME

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18EC33

## Third Semester B.E. Degree Examination, Jan./Feb. 2021 Electronic Devices

Time: 3 hrs.

Max. Marks: 100

*Note: Answer any FIVE full questions, choosing ONE full question from each module.*

### Module-1

- 1 a. Write the figures of the resulting orbitals when isolated atoms brought together and explain the characteristics. (10 Marks)
- b. Obtain the relationship between mobility and hall coefficient in a p-type bar placed in a magnetic field in the Z-direction. (10 Marks)

OR

- 2 a. Derive the equation which relates current density and mobility in a semiconductor in an applied electric field. (10 Marks)
- b. A silicon bar  $2\mu\text{m}$  long and  $200\mu\text{m}^2$  in cross sectional area is doped with  $1.5 \times 10^{17}/\text{cm}^3$  phosphorus. Find the current at 300K with 30V applied voltage. How long does it take an average electron to drift  $2\mu\text{m}$  in pure silicon at an electric field of  $80\text{V}/\text{cm}$ ? Also calculate the time required at  $10^5\text{V}/\text{cm}$ . Assume mobility of electrons is  $0.1350\text{m}^2/\text{Vsec}$ . Also assume that saturation of electron drift velocity for silicon is  $10^7\text{ cm/s}$  for the electric field above  $10^5\text{ V/cm}$ . (10 Marks)

### Module-2

- 3 a. Show the effect of bias at a pn junction on transition region width, electric field, electrostatic potential, energy band diagram partic flow and current direction under the following conditions:
  - i) Equilibrium
  - ii) Forward bias
  - iii) Reverse bias. (10 Marks)
- b. Illustrate the care and issues to be considered in the design of solar cells. (10 Marks)

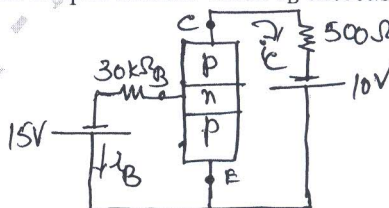
OR

- 4 a. Explain Avalanche break down and obtain equation for the electron multiplication factor. (10 Marks)
- b. Derive the relationship between the open circuit voltage and optic generation rate starting from the expression for the optically generated illuminated pn junction. (10 Marks)

### Module-3

- 5 a. Show the hole and electron flow in a pnp transistor with proper biasing. (08 Marks)
- b. For the circuit shown in Fig.Q.5(b) calculate  $\beta$ ,  $I_B$  and  $I_C$ . Given that  $\tau_p = 18\mu\text{s}$ , and  $\tau_t = 0.2\mu\text{s}$ . What happens to the output current when  $I_B$  increases and  $\beta$  increases? (06 Marks)

Fig.Q.5(b)



(06 Marks)

- c. Explain the concept of base narrowing in a  $p^+ - n - p^+$  transistor. (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and/or equations written eg, 42+8 = 50, will be treated as malpractice.

OR

- 6 a. Obtain the Ebers-Moll equations and represent the same in the model form. (12 Marks)  
 b. Describe the switching effects in a CE transistor circuit. (08 Marks)

**Module-4**

- 7 a. Analyze the effect on gate-to-channel-space charge region and IV characteristics for the following conditions in a JFET:  
 i) Zero gate voltage of a small drain voltage  
 ii) Zero gate voltage of a large drain voltage  
 iii) Small  $V_{DS}$  value and small reverse-biased gate voltage. (10 Marks)
- b. Draw the energy band diagram in an MOS capacitor structure for the following cases:  
 i) p-type substrate for a positive gate bias  
 ii) p-type substrate for a large positive gate bias  
 iii) n-type substrate for a positive gate bias. (10 Marks)

OR

- 8 a. Write the small signal equivalent circuit of a JFET, ideal low frequency small signal equivalent circuit and ideal equivalent circuit including  $r_s$ . (10 Marks)  
 b. Show the channel formation in the MOS structure and  $I_D$  versus  $V_{DS}$  curve for the following cases:  
 i)  $V_{gs} > V_t$  and small  $V_{DS}$  value  
 ii)  $V_{gs} > V_t$  and large  $V_{DS}$  value  
 iii)  $V_{gs} > V_t$  and  $V_{DS} = V_{DS}(\text{sat})$  (10 Marks)

**Module-5**

- 9 a. What are the fabrication steps used in the fabrication of pn junctions? (10 Marks)  
 b. With figures, describe the complementary MOS structure. (10 Marks)

OR

- 10 a. Illustrate the evolution of integrated circuits. (10 Marks)  
 b. Explain the formation of resistors in integrated circuits. (10 Marks)

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