CBCS SCHEME

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17EE34

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. For the clipper limit shown in Fig Q1(a). Find V_0, sketch the V_0 waveform and also draw the transfer characteristics

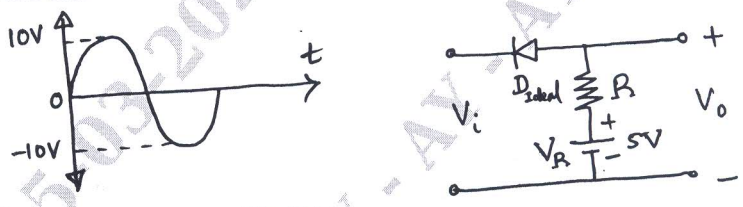

Fig Q1(a) **(07 Marks)**

b. With a neat circuit diagram, explain the operation fixed bias circuit. **(07 Marks)**

c. What is biasing of a transistor? Explain the requirements of biasing circuits. **(06 Marks)**

OR

2 a. Find the operating point for the voltage divider bias circuit with $\beta = 80$ and $V_{BE} = 0.6V$. Find the new operating point when β changes to 100 and V_{BE} changes to 0.25V. Consider, $V_{CC} = 15V$, $R_1 = 100K\Omega$, $R_2 = 18K\Omega$, $R_c = 4.7K\Omega$ and $R_E = 1K\Omega$. **(10 Marks)**

b. Obtain the expression for stability factor (S_{Ico}) for collector to base bias circuit. **(05 Marks)**

c. Explain the operation of a transistor as a switch. **(05 Marks)**

Module-2

3 a. Define h-parameters. Obtain the expression for current gain, voltage gain, input resistance and output resistance for CE configuration of BJT using h-parameters. **(10 Marks)**

b. For the emitter follower circuit shown in Fig Q3(b). Calculate z_i, z_o, A_v and A_i. Take the h-parameter of the transistor to be $h_{ie} = 1.1K\Omega$, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 24\ \mu A/v$

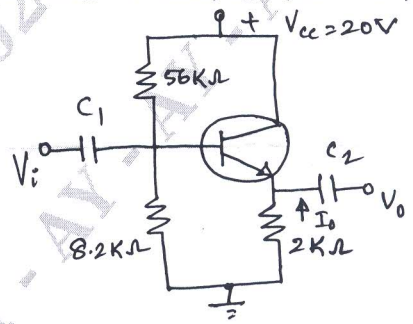

Fig Q3(b) **(06 Marks)**

c. A transistor in CE mode has h-parameters, $h_{ie} = 1100\Omega$, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 99$ and $h_{oe} = 25\mu A/v$. Determine equivalent CB parameters. **(04 Marks)**

OR

4 a. For the common base circuit shown in Fig Q4(a), the transistor parameters are $h_{ib} = 22\Omega$, $h_{rb} = 2.9\times10^{-4}$, $h_{fb} = -0.98$ and $h_{ob} = 0.49$ μA/v. Calculate the values of the input resistance, output resistance, current gain and voltage gain for the given circuit.

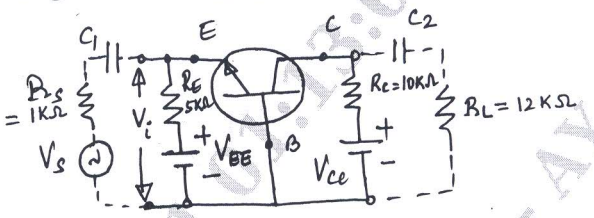

Fig Q4(a) **(10 Marks)**

b. State and prove Miller's theorem. **(10 Marks)**

Module-3

5 a. Explain the need for cascading amplifier. Draw and explain block diagram of n-stage cascaded amplifier. **(06 Marks)**

b. Compare the different types coupling methods used in multistage amplifiers. **(08 Marks)**

c. With the help of a neat circuit diagram, explain the working of a Darlington emitter follower. **(06 Marks)**

OR

6 a. Define Negative and Positive feedback. With the help of block diagram, explain the concept of feedback amplifier. **(07 Marks)**

b. Derive the expression for Z_{if} and Z_{of} for a voltage series feedback amplifier. **(08 Marks)**

c. An amplifier having a voltage gain of 60dB uses $1/20^{th}$ of it output in negative feedback. Calculate to the gain with feedback, the percentage change in gain without and with feedback consequent on 50% change in g_m (transfer or mutual conductance). **(05 Marks)**

Module-4

7 a. Explain the operation of a class-B push pull power amplifier. Prove that the maximum efficiency of a class – B configuration is 78.5%. **(10 Marks)**

b. State and explain Barkhausen criterion for sustained Oscillations. **(05 Marks)**

c. Explain the features of power amplifiers. **(05 Marks)**

OR

8 a. Draw the circuit of wein bridge oscillator and derive an expression for frequency of oscillator. **(10 Marks)**

b. Explain the operation of class A transformer coupled power amplifier and prove that the maximum efficiency is 50%. **(10 Marks)**

Module-5

9 a. Discus the construction, working and characteristics of an n-channel JFET. **(10 Marks)**

b. Give the comparison between the following :
i) BJT and FET ii) JFET and MOSFET iii) D-MOSFET and E-MOSFET. **(10 Marks)**

OR

10 a. Discuss the construction, working and characteristics of an enhancement type MOSFET [E-MOSFET]. **(10 Marks)**

b. With necessary equivalent circuit, obtain the expression for voltage gain, input impedance and output impedance of a Fixed biased common source – JFET amplifier. **(10 Marks)**

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