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CBCS SCHEME

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15EE34

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Show the output waveform for the network shown in Fig Q1(a). If the peak value of ac input is 15V. Show all the voltage levels in the output. Assume ideal diode.

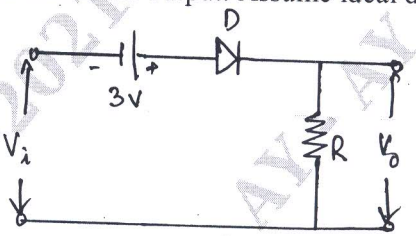

Fig Q1(a)

(05 Marks)

b. With circuit diagram, explain emitter stabilized bias circuit. Write the necessary equations. **(05 Marks)**

c. For the circuit shown in Fig Q1(c), calculate I_C, V_B and $S_{(ICO)}$. Given $\beta = 100$ and $V_C = 12V$.

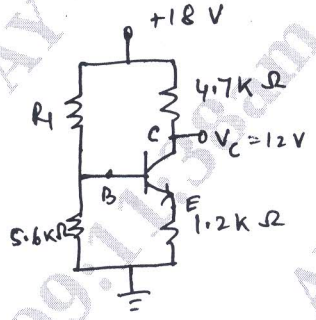

Fig Q1(c)

(06 Marks)

OR

2 a. Explain the operation of positive clamper circuit. **(05 Marks)**

b. Consider a fixed bias circuit of a BJT. Obtain expression for stability factors $S_{(I_{CO})}$, $S_{(V_{BE})}$ and S_β. **(06 Marks)**

c. Design the emitter bias circuit shown in Fig Q2(c), for operating point given as $V_{CEQ} = 10V$, $I_{CQ} = 1.5mA$.

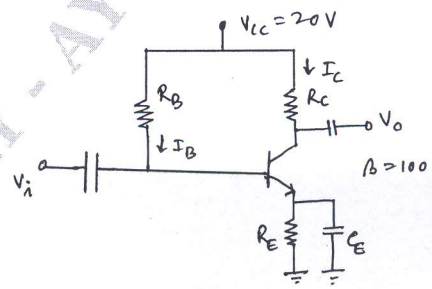

Fig Q2(c)

(05 Marks)

Module-2

3 a. Draw the circuit diagram of common emitter configuration of BJT fixed bias amplifier. Derive expression for A_V, A_i, Z_i and Z_o. **(10 Marks)**

b. A 2 stage cascaded amplifier system is built with stage voltage gains 25 and 40. Both stages have the same bandwidth of 220KHz with identical lower cutoff frequency of 500Hz. Find overall gain band width product. **(06 Marks)**

OR

4 a. Describe Miller effect and derive an equation for Miller input and output capacitances. **(06 Marks)**

b. For the common base configuration shown in Fig 4(b), the transistor parameters are $h_{ib} = 22\Omega$, $h_{fb} = -0.98$, $h_{ob} = 0.49\,\mu A/V$, $h_{rb} = 2.9 \times 10^{-4}$. Calculate the values of input resistance, output resistance, current gain and voltage gain for the given circuit.

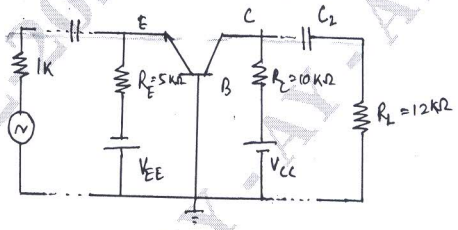

Fig Q4(b) **(10 Marks)**

Module-3

5 a. For a Darlington emitter follower circuit $R_B = 1.2\mu\Omega$, $r_i = 5k\Omega$, $\beta_D = 8000$, $V_{BE} = 1.6V$, $R_E = 330\Omega$. Calculate Z_i, Z_o, A_i and A_V. Derive the necessary equations. **(08 Marks)**

b. Derive expression for output resistance for a current shunt feedback amplifier. **(08 Marks)**

OR

6 a. Mention the types of feedback connections; draw their block diagram indicating input and output signals. **(04 Marks)**

b. If an amplifier has a bandwidth of 200KHz and a voltage gain of 80, what will be the new bandwidth and gain if a negative feedback of 5% introduced? **(04 Marks)**

c. Explain the operation of cascade connection with the help of neat diagram. **(08 Marks)**

Module-4

7 a. Draw the circuit diagram and explain the operation of class B push pull amplifier. **(08 Marks)**

b. Explain the characteristics of quartz crystal. **(04 Marks)**

c. In a Hartley oscillator, $L_1 = 20\mu H$, $L_2 = 2mH$, C is variable. Find the range of C if frequency is to be varied from 1.5MHz to 2.5MHz. **(04 Marks)**

OR

8 a. Calculate the maximum efficiency of the class A amplifier as shown in Fig Q8(a). Assume transformer has 80% efficiency. **(08 Marks)**

$V_{CC} = +13V$
$R_E = 1k\Omega$
$\beta = 25$

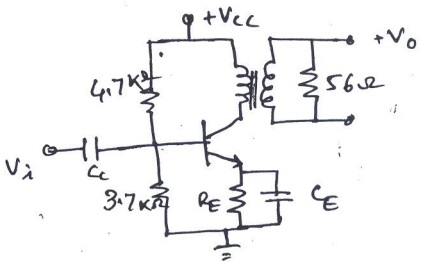

Fig Q8(a)

b. What is Barkhausen criterion for sustained oscillations? Explain basic principle of operation of oscillator. **(04 Marks)**

c. With circuit diagram explain RC phase shift oscillator using BJT. **(04 Marks)**

Module-5

9 a. With necessary equivalent circuit derive the expression for A_v, Z_{in} and Z_o for a fixed bias JFET amplifier. **(08 Marks)**

b. Explain depletion and enhancement types MOSFETs and their characteristics. **(08 Marks)**

OR

10 a. Calculate the transconductance g_m of a JFET having values of $I_{DSS} = 12mA$, $V_P = -4V$ at bias points i) $V_{GS} = 0V$ ii) $V_{GS} = -1.5V$. **(04 Marks)**

b. List the differences between JFET and MOSFET. **(05 Marks)**

c. Explain voltage divider biasing of n channel enhancement types MOSFET. **(07 Marks)**

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