CBCS SCHEME

15MT62

Sixth Semester B.E. Degree Examination, Aug./Sept. 2020
Embedded Systems (ARM)

Time: 3 hrs.   Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1   a. List and explain the major design rules used for RISC design philosophy. **(08 Marks)**
    b. With a neat sketch, explain current program status Register. **(08 Marks)**

OR

2   a. Explain the following Embedded system hardware components
       i) AMBA Bus Protocol   ii) Memory. **(10 Marks)**
    b. Explain Exceptions, interrupts and vector table in ARM. **(06 Marks)**

Module-2

3   a. Explain the following ARM instructions with example
       i) MOVE instruction   ii) Arithmetic instruction   iii) Comparison instruction. **(08 Marks)**
    b. Explain the following ARM instruction
       i) Coprocessor instruction   ii) SWAP instruction   iii) Logical instruction. **(08 Marks)**

OR

4   a. Explain the following :
       i) ARM-Thumb interworking   ii) Multiple register load store instruction. **(08 Marks)**
    b. Explain the following Thumb instruction
       i) Branch instruction   ii) Stack instruction. **(08 Marks)**

Module-3

5   a. Explain the parallel operation performed in instruction scheduling in ARM processor. Also explain One cycle interlock caused by load use. **(08 Marks)**
    b. Explain load scheduling with preloading with example code. **(08 Marks)**

OR

6   Explain the following :
    i) Allocating variables to register number ii) Looping constructs. **(16 Marks)**

Module-4

7   a. Explain Different cache policies. **(10 Marks)**
    b. Differentiate between physical and logical cache. **(06 Marks)**

OR

8   a. Explain the architecture of cache. **(08 Marks)**
    b. With the neat figure, explain how memory maps to direct mapped cache. **(08 Marks)**

Module-5

9   Explain the following :
    i)   Arm processor mode and exceptions
    ii) vector table
    iii) Exception priorities
    iv) Link register offsets. **(16 Marks)**

OR

10 a. Explain non-nested interrupt handling scheme. **(08 Marks)**
    b. Explain nested interrupt handling scheme. **(08 Marks)**

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