CBCS SCHEME

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15MT35

Third Semester B.E. Degree Examination, Aug./Sept. 2020
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the operation of PN junction diode with V.I characteristics under different biasing conditions. **(08 Marks)**

b. Explain the operation of zener diode as a voltage regulator with neat circuit diagrams. **(08 Marks)**

OR

2 a. Explain the operation of a diode as a switch and with neat diagram of switching response. **(08 Marks)**

b. Explain bridge rectifier with capacitor filter with neat waveforms and derive the expression for ripple factor. **(08 Marks)**

Module-2

3 a. Explain the first order high pass Butterworth filter and derive the gain equation. **(08 Marks)**

b. Design a lawpass second order Butterworth filter with cutoff frequency 1KHz and draw the frequency response. **(08 Marks)**

OR

4 a. With neat diagram, explain the operation of RC phase shift oscillator and derive the expression for following oscillators **(08 Marks)**

b. Explain the operation of wien bridge oscillator and derive the expression for frequency of oscillators. **(08 Marks)**

Module-3

5 a. Explain Investing comparator with neat input and output waveform if V_{ref} is Positive and Negative. **(08 Marks)**

b. Explain the operation of Schmitt trigger with neat waveforms and hysteresis curve. **(08 Marks)**

OR

6 a. Explain the operation of 555 timer as a astable multivibrator with neat diagram and waveforms. **(08 Marks)**

b. Explain the operation of 555 timer as a monostable multivibrator with neat diagrams. **(08 Marks)**

Module-4

7 a. Explain the operation of AND and OR logic using toggle switches, truth table, timing diagram and diode logic. **(08 Marks)**

b. Explain emitter coupled logic with neat diagram. **(08 Marks)**

OR

8 a. With neat diagram and truth tables explain RS and JK filpflops. **(08 Marks)**

b. Explain the operation of modulo - 16 ripples down counter with schematic, timing and state diagrams. **(08 Marks)**

Module-5

9 a. Explain the operation of multiplexer and demultiplexers with truth task and logic diagrams. **(08 Marks)**

b. Design a 4 × 16 decodes with two 3 × 8 decoders and draw the truth table. **(08 Marks)**

OR

10 a. With neat circuit diagram, explain weighted resistor DAC with an example. **(08 Marks)**

b. Explain the operations of successive approximation ADC with necessary functional diagrams. **(08 Marks)**

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