CBCS SCHEME

USN [ ] 18MT36

Third Semester B.E. Degree Examination, Aug./Sept. 2020
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define Computer. Explain different types of computers. **(08 Marks)**
b. Discuss the block diagram of basic functional units of computer. **(06 Marks)**
c. With neat diagram, explain connection between the processor and the memory. **(06 Marks)**

OR

2 a. Explain the role of each parameter in the basic performance equation of the computer. **(04 Marks)**
b. Explain basic instruction types with example. **(06 Marks)**
c. With neat diagram, explain byte addressability Big-endian and Little-endian assignment. **(10 Marks)**

Module-2

3 a. Explain addressing modes with example. **(10 Marks)**
b. Explain with neat diagram bus connection for processor, keyboard and display. **(05 Marks)**
c. Explain assembler directive i) EQU ii) ORIGIN iii) DATAWORD iv) RESERVE v) END. **(05 Marks)**

OR

4 a. Define Stack. Write assembly instruction for safe push operation and safe pop operation. **(08 Marks)**
b. Explain with neat diagram, logical and arithmetic shift instructions. **(12 Marks)**

Module-3

5 a. Explain with neat diagram, I/O interface for an input device. **(06 Marks)**
b. Write a program that reads one line from keyboard stores it in memory buffer and echoes it back to the display. **(06 Marks)**
c. Define interrupt. Explain with neat diagram interrupt priority scheme. **(08 Marks)**

OR

6 a. List the sequence of events involved in handling an interrupt request from a single device. **(05 Marks)**
b. With neat diagram, explain the implementation of interrupt priority using individual request and acknowledge line. **(05 Marks)**
c. Define bus arbitration. Explain two approaches of bus arbitration. **(10 Marks)**

Module-4

7 a. With neat diagram, explain connection of the memory to the processor. **(06 Marks)**
b. Explain internal organization of a 2m × 8 dynamic memory chip. **(08 Marks)**
c. Differentiate between the direct mapped cache and associative mapped cache. **(06 Marks)**

OR

8	a.	Explain synchronous DRAMs along with burst read of length 4 in a SDRAM.	**(10 Marks)**
	b.	With neat diagram, explain virtual memory organization.	**(05 Marks)**
	c.	Explain read and write operation in static memory.	**(05 Marks)**

Module-5

9	a.	With neat diagram, explain single bus organization of the data path inside a processor.	**(10 Marks)**
	b.	Write the control sequence for an unconditional branch instruction.	**(05 Marks)**
	c.	Discuss the action needed to execute instruction MOV (R1), R2.	**(05 Marks)**

OR

10	a.	With neat diagram, explain three bus organization of the data path.	**(10 Marks)**
	b.	Write the control sequence for execution of the instruction Add (R3), R1.	**(10 Marks)**

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