CBCS SCHEME

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17MT36

Third Semester B.E. Degree Examination, Aug./Sept.2020
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With a neat diagram, discuss the basic operational concept of a computer. **(08 Marks)**

b. What is straight line sequencing? Write a straight line program segment that appears in memory for adding n numbers. **(08 Marks)**

c. What are condition code flags? Write four commonly used flags. **(04 Marks)**

OR

2 a. Explain Little-endian and Big-endian assignment with neat diagram ad example. **(08 Marks)**

b. What are basic instruction types? Explain with example. **(08 Marks)**

c. Explain three different systems used for representing signed number. **(04 Marks)**

Module-2

3 a. What are addressing modes? Explain any three addressing modes with example. **(10 Marks)**

b. What is subroutine? Explain subroutine linkage method with an example. **(10 Marks)**

OR

4 a. What are assembler directives? Explain with example program. **(10 Marks)**

b. Explain the following:
(i) Logical shift left (ii) Logical shift right (iii) Rotate left
(iv) Rotate right (v) Arithmetic shift right **(10 Marks)**

Module-3

5 a. Explain with a neat diagram non interrupt request are handled using Dairy chain and priority groups. **(10 Marks)**

b. With a neat detailed timing diagram, explain how input transfer happens on synchronous bus. **(10 Marks)**

OR

6 a. What is DMA? Explain in detail. **(06 Marks)**

b. What is interrupt nesting? Explain with a neat diagram the implementation of interrupt priority using individual interrupt request and acknowledgement lines. **(08 Marks)**

c. Explain a general 8-bit parallel interface with a neat diagram. **(06 Marks)**

Module-4

7 a. Draw the organization of 16 × 8 memory chip and explain its working. **(08 Marks)**

b. Explain the operation of synchronous DRAM with a neat block diagram. **(08 Marks)**

c. What is virtual memory technique? Draw neat diagram of virtual memory organization. **(04 Marks)**

OR

8 a. Draw the organization of 1K × 1 memory chip and explain its working. **(08 Marks)**

b. Explain asynchronous DRAM operation with a neat block diagram. **(08 Marks)**

c. Explain write through protocol and write back protocol with respect to cache memory. **(04 Marks)**

Module-5

9 a. Explain single bus organization of the data path inside a processor with a neat diagram. **(08 Marks)**

b. Write the control sequence for execution of the instruction Add (R_3), R_1. **(06 Marks)**

c. With a neat diagram, explain hardwired control unit organization. **(06 Marks)**

OR

10 a. Explain multiple bus organization of the datapath with a neat diagram. **(08 Marks)**

b. Describe microprogrammed control unit organization with a neat diagram. **(08 Marks)**

c. Write a control sequence for an unconditional branch instruction. **(04 Marks)**

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