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10EC63

Sixth Semester B.E. Degree Examination, Aug./Sept. 2020
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any THREE full questions from Part-A and any TWO full questions from Part-B.***

PART – A

1 a. Derive an expression for drain current of a MOSFET in different regions of operation. **(05 Marks)**

b. Explain how the MOSFET can be used as an amplifier and as a switch. **(05 Marks)**

c. Explain different biasing methods in MOS amplifier circuits. **(10 Marks)**

2 a. Draw the development of the T-equivalent circuit model for the MOSFET. **(05 Marks)**

b. The NMOS and PMOS transistors in the circuit shown in Fig. Q2 (b) are matched with $K'_n\left(\frac{\omega_n}{L_n}\right) = K'_P\left(\frac{\omega_P}{L_P}\right) = 1\frac{mA}{V^2}$ and $V_{tn} = -V_{tp} = 1$ V. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP} and the voltage V_0 for $V_I = 0$ V, +2.5V and -2.5V. **(05 Marks)**

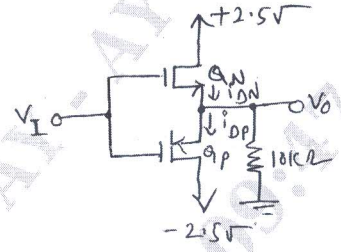

Fig. Q2 (b)

c. For a common gate amplifier with $g_m = 1$ mA/V and $R_D = 15$ KΩ. Find R_{in}, R_{out}, AV_O, A_V and G_V for $R_L = 15$ KΩ and $R_{sig} = 50$ Ω. What will the overall voltage can become for $R_{sig} = 1$ KΩ, 10 KΩ and 100 KΩ. **(10 Marks)**

3 a. What is MOSFET scaling? Explain about short channel effect due to scaling. **(05 Marks)**

b. Explain with neat diagram of Wilson MOS mirror. **(05 Marks)**

c. Given $V_{DD} = 3$V and $I_{REF} = 100$ μA it is required to design a basic MOSFET constant current source to obtain an output current whole nominal value is 100 μA. Find R if Q_1 and Q_2 are matched and have channel length's of 1 μm, channel width's of 10 μm, $V_t = 0.7$ V and $K'_n = 200$ μA/V^2. What is the lowest possible value of V_0? Assuming that for this process technology the early voltage $V'_A = 20$ V/μm, find the output resistance of the current source. Also, find the change in output current resulting from a+1-V change in V_0. **(05 Marks)**

d. Draw the BJT constant current source circuit and explain it. **(05 Marks)**

4 a. In common gate amplifier with active load, obtain 3-dB frequency for using open circuit time constants. Draw the circuit required for determining R_{gs} and R_{gd}. **(10 Marks)**

b. Consider a source follower circuit, specified as follows : W/L = 7.2 μm/0.36 μm, $I_D = 100$ μA, $g_m = 1.25$ mA/V, $\chi = 0.2$, $r_0 = 20$ KΩ, $R_{sig} = 20$ KΩ, $R_L = 10$ KΩ, $C_{gs} = 20$ fF, $C_{gd} = 5$ fF, $C_L = 15$ fF. Find three capacitances C_{gd}, C_{gs} and C_L. Find τ_H and the percentage contribution to it from each of three capacitances. Find f_H. **(10 Marks)**

5 a. Draw the two stage Op-Amp CMOS OpAmp configuration and briefly explain obtain overall open loop gain. **(08 Marks)**

b. The differential amplifier in figure uses transistors with $\beta = 100$. Evaluate the following:

(i) The input differential resistance R_{id}.

(ii) The overall differential voltage gain V_0/V_{sig} (Neglect the effect of r_0).

(iii) The worst case common mode gain if the two collector resistances are accurate to within $\pm 1\%$.

(iv) The CMRR in dB.

(v) The input common mode resistance (assuming that the early voltage $V_A = 100$ V)

(12 Marks)

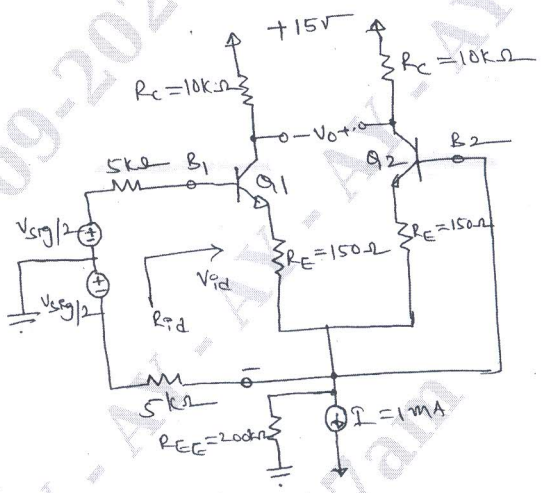

Fig. Q5 (b)

PART – B

6 a. Explain briefly with expressions the properties of Negative feedback. **(10 Marks)**

b. Explain about Shunt-Shunt feedback amplifier with diagram and obtain the expression for input impedance and output impedance. **(10 Marks)**

7 a. Explain instrumentation amplifier with neat circuit diagram. **(05 Marks)**

b. Use the superposition principle to find the output voltage of the circuit shown in Fig. Q7 (b). **(05 Marks)**

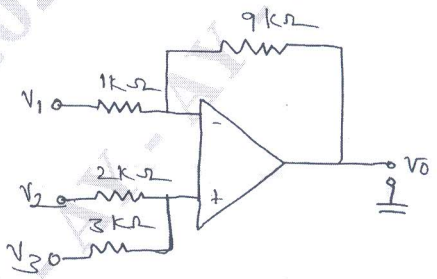

Fig. Q7 (b)

c. Explain logarithmic and antilogarithmic amplifiers with neat diagrams. **(10 Marks)**

8 a. Explain the dynamic operation of a CMOS inverter. **(10 Marks)**

b. Sketch a CMOS logic circuit that realizes the function $Y = \overline{ABC + DE}$, using AOI gate. **(04 Marks)**

c. Explain charge sharing problem in dynamic 3-input NAND circuits. **(06 Marks)**

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