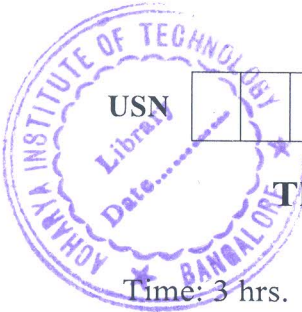


# CBCS SCHEME



15EC32

**Third Semester B.E. Degree Examination, Aug./Sept. 2020**

## Analog Electronics

Time: 3 hrs.

Max. Marks: 80

**Note: Answer any FIVE full questions, choosing ONE full question from each module.**

### Module-1

- 1 a. Derive an expression for  $A_v$ ,  $Z_i$  and  $Z_o$  for CE fixed bias using hybrid equivalent model. (08 Marks)
- b. With a neat circuit explain hybrid  $\pi$  model for a transistor in CE configuration. (08 Marks)

OR

- 2 a. Derive an expression for  $Z_i$ ,  $Z_o$  and  $A_v$  for emitter – Follower configuration using  $r_e$  model. (08 Marks)
- b. For the network shown in Fig Q2(b). Determine :  
 i)  $r_e$       ii)  $Z_i$       iii)  $Z_o$  ( $r_o = \alpha\Omega$ )      iv)  $A_v$  ( $r_o = \alpha\Omega$ )      v)  $A_i$  ( $r_o = \alpha\Omega$ ).

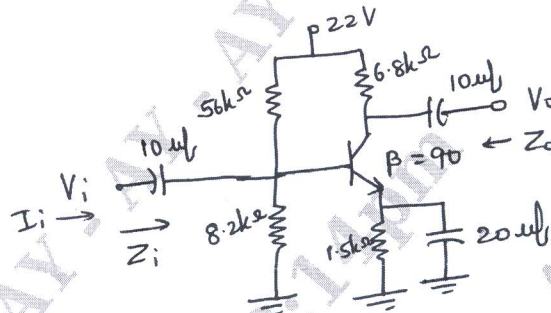


Fig Q2(b)

(08 Marks)

### Module-2

- 3 a. Derive an expression for  $Z_i$ ,  $Z_o$  and  $A_v$  of FET self bias configuration with bypassed  $R_s$ . (08 Marks)
- b. Explain the construction and working principle of n-channel depletion type MOSFET and draw the characteristic curves. (08 Marks)

OR

- 4 a. The fixed bias configuration of Fig Q4(a) has an operating point defined by  $V_{GSQ} = -2V$  and  $I_{DQ} = 5.625mA$  with  $I_{DSS} = 10mA$  and  $V_p = -8V$ . Determine :  
 i)  $g_m$       ii)  $r_d$       iii)  $Z_i$       iv)  $Z_o$       v)  $A_v$ .

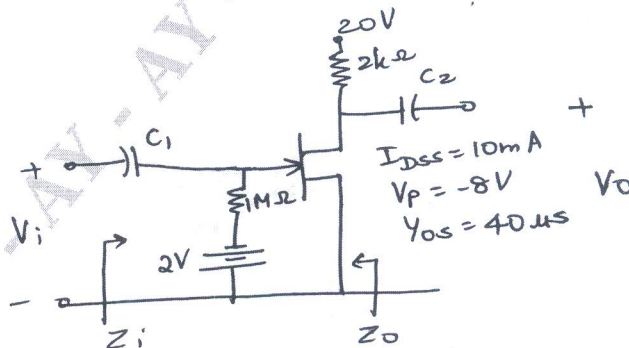


Fig Q4(a)

(08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

- b. Draw the JFET common drain configuration circuit. Derive  $Z_i$ ,  $Z_o$  and  $A_v$  using small signal model. (08 Marks)

**Module-3**

- 5 a. The i/p power to a device is 10,000w at a voltage of 1000V. The output power is 500W and the output impedance is  $20\Omega$ .  
 i) Find power gain in db  
 ii) Find voltage gain in db  
 iii) Find input impedance. (06 Marks)
- b. Describe Miller's effect and derive an equation for Miller input and output capacitance. (10 Marks)

**OR**

- 6 a. Explain high frequency response of FET amplifier. (06 Marks)
- b. Determine  $A_v$ ,  $Z_i$ ,  $A_{vs}$ ,  $F_{LS}$  for the low frequency response of the BJT amplifier circuit shown in Fig Q6(b). Assume  $r_o = \alpha$ .

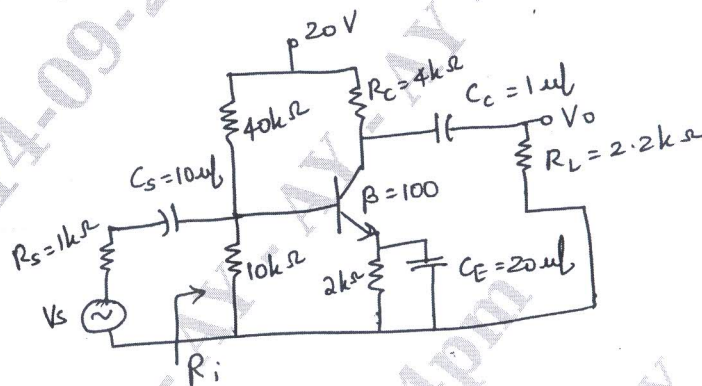


Fig Q6(b)

(10 Marks)

**Module-4**

- 7 a. Explain with neat circuit diagram the operation of transistor Colpitt's oscillator. (08 Marks)
- b. What are the effects of negative feedback in an amplifier? Show how bandwidth of an amplifier increases with negative Feedback. (08 Marks)

**OR**

- 8 a. Mention the types of Feedback connections. Draw their block diagrams indicating i/p and o/p signal. (08 Marks)
- b. With a neat circuit and waveforms, explain the working operation of UJT relaxation oscillator. (08 Marks)

**Module-5**

- 9 a. Explain the operation of class B push pull amplifier and show that maximum conversion  $\eta$  is 78.5% (10 Marks)
- b. The Following distortion readings are available for a power amplifier  $D_2 = 0.1$ ,  $D_3 = 0.02$ ,  $D_4 = 0.01$  with  $I_1 = 4A$ ,  $R_c = 8\Omega$ .  
 i) Calculate the THD  
 ii) Determine the fundamental power component  
 iii) Calculate the total power. (06 Marks)

**OR**

- 10 a. Explain series voltage regulator using transistor. (08 Marks)
- b. Explain series Fed class A power amplifier. Show that its maximum conversion  $\eta$  is 25%. (08 Marks)

\* \* \* \* \*