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18EC34

Third Semester B.E. Degree Examination, Aug./Sept.2020
Digital System Design

Time: 3 hrs.   Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Place the following equations into proper canonical forms:
   i) $f(abc) = a\overline{b} + a\overline{c} + bc$
   ii) $f(abcd) = (a + \overline{b})(a + \overline{b} + d)$ **(06 Marks)**

   b. Identify all the prime implicants and essential prime implicants of the Boolean function using K-map.
   $f(abcd) = \Sigma(0, 1, 2, 5, 6, 7, 8, 9, 10, 13, 14, 15)$ **(06 Marks)**

   c. Find the minimal sum and minimal product for the function using K-map.
   $f(abcd) = \Sigma(6, 7, 9, 10, 13) + \Sigma d(1, 4, 5, 11, 15)$ **(08 Marks)**

OR

2 a. Represent the number of days in a month for a non-leap year by a truth table, indicating the output of invalid input if any by '0'.   **(05 Marks)**

   b. Find all the prime implicants of the function using Quine-McClusky method.
   $f(abcd) = \Sigma(7, 9, 12, 13, 14, 15) + d(4, 11)$ **(10 Marks)**

   c. Simplify the given Boolean equation using K-map:
   $f(abcd) = \pi(1, 2, 3, 4, 9, 10) + \pi d(0, 14, 15)$ **(05 Marks)**

Module-2

3 a. Implement full subtractor using 74138 decoder.   **(06 Marks)**

   b. Design 2-bit magnitude comparator.   **(08 Marks)**

   c. Implement Boolean function using 8:1 MUX treat a, b, c as select lines:
   $f(abcd) = \Sigma(0, 1, 5, 6, 7, 9, 10, 15)$ **(06 Marks)**

OR

4 a. Implement the Boolean function $f(abcd) = \Sigma(0, 2, 4, 5, 7, 9, 10, 14)$ using multiplexers with two 4:1 MUX with variable a, d connected to their select lines in the first level and one 2:1 MUX with variable 'C' connected to its select lines in the second level.   **(10 Marks)**

   b. Implement Boolean function $f(abcd) = \Sigma(4, 5, 7, 8, 10, 12, 15)$ using 4:1 MUX and external gates:
   (i)   a, b are connected to select line $a_1 \, a_0$ respectively
   (ii) c, d are connected to select lines $a_1 \, a_0$ respectively.   **(10 Marks)**

Module-3

5 a. Explain the operation of switch debouncer using SR latch with the help of circuit and waveforms.   **(07 Marks)**

   b. Explain Master Slave JK F/F with the help of circuit diagram and waveforms.   **(07 Marks)**

   c. Design a 4-bit binary ripple-up counter using negative edge triggered JK flip-flop. **(06 Marks)**

OR

6 a. Explain positive edge triggered D-flip-flop with the help of circuit diagram and waveforms.
(08 Marks)

b. Design a 4-bit universal shift register using positive edge triggered D-flip-flop and multiplexers to operate as indicated below:

Mode select	Operation
00	Hold
01	Right shift
10	Left shift
11	Parallel load

(08 Marks)

c. Write the difference between ripple counter and synchronous counter.
(04 Marks)

Module-4

7 a. Design 3 bit synchronous up-counter using J-K flip-flop. (10 Marks)

b. Design a mod-6 synchronous counter using D-flip flop for the sequence 0-2-3-6-5-1.
(10 Marks)

OR

8 a. Draw and explain block diagram of Moore model and mealy model. (06 Marks)

b. Design a synchronous circuit using positive edge triggered J-K flip-flop with minimal combinational gating to generate the sequence:
$0 - 1 - 2 - 0$ if input $x = 0$
$0 - 2 - 1 - 0$ if input $x = 1$
Provide an output which goes high to indicate the non-zero state in the sequence $0 - 1 - 2 - 0$.
(08 Marks)

c. Design mod-5 synchronous counter using TF/F. (06 Marks)

Module-5

9 a. A sequential circuit has one input (x) and one output (z) the circuit examines groups of four consecutive inputs and produces an output z = 1 if the input sequence 0101 or 1001 occurs. The circuit resets after every four inputs. Find the mealy state graph typical sequence is 0101 0010 1001 0100. (10 Marks)

b. Explain with block diagram design and serial Adder with accumulator. (10 Marks)

OR

10 a. Write a short note on 4×4 bit binary parallel multiplication. (10 Marks)

b. List the guide lines for construction of state graphs. (10 Marks)

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