CBCS SCHEME

Third Semester B.E. Degree Examination, Aug./Sept.2020
Analog Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Derive expressions for Z_i, Z_o, A_v and A_I for common emitter fixed bias configuration using hybrid equivalent model. **(10 Marks)**

   b. Draw and explain the hybrid-π model of transistor in CE configuration mentioning significance of each component in model. **(06 Marks)**

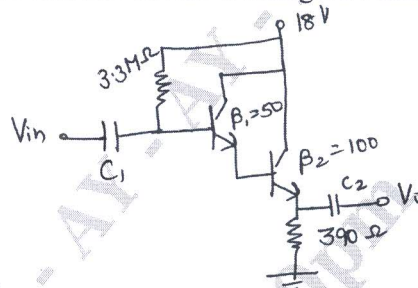   c. Calculate DC bias voltage and currents for the Darlington configuration shown in Fig.Q1(c).

Fig.Q1(c) **(04 Marks)**

OR

2 a. Derive the expression for Z_i, Z_o and A_v for emitter follower configuration using r_e model. **(10 Marks)**

   b. Define h parameters and derive h parameters model of CE-BJT. **(10 Marks)**

Module-2

3 a. Explain the construction and working principle of n-channel JFET and draw the characteristics. **(08 Marks)**

   b. Derive an expression for Z_i, Z_o and A_v of FET self bias configuration with bypassed R_S. **(08 Marks)**

   c. Distinguish between JFET and MOSFET. **(04 Marks)**

OR

4 a. Draw the JFET common gate configuration circuit. Derive Z_i, Z_o and A_v using small signal model. **(10 Marks)**

   b. The fixed bias configuration of Fig.Q4(b) has an operating point defined by $V_{GSQ} = -2V$ and $I_{DQ} = 5.625$ mA with $I_{DSS} = 10$ mA and $V_P = -8V$. Determine : (i) g_m (ii) r_d (iii) Z_i (iv) Z_o (v) A_v
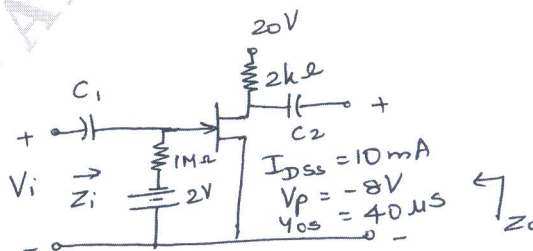

Fig.Q4(b) **(10 Marks)**

Module-3

5 a. Describe Miller effect and derive an equation for miller input and output capacitance.

(10 Marks)

b. Explain high-frequency response of FET amplifier and derive expression for cut off frequencies defined by input and output circuits (f_{Hi} and f_{Ho}). (10 Marks)

OR

6 a. Determine the lower cut off frequencies for the voltage divider bias BJT amplifier with $C_S = 10$ μf, $C_C = 1$ μf, $C_E = 20$ μf, $R_S = 1$ kΩ, $R_1 = 40$ kΩ, $R_2 = 10$ kΩ, $R_E = 2$ kΩ, $R_0 = 4$ kΩ, $R_L = 2.2$ kΩ, $β = 100$, $r_0 = α Ω$, $V_{CC} = 20$ V. (10 Marks)

b. Obtain the expressions for overall lower and higher cut-off frequencies for a multistage amplifier. (10 Marks)

Module-4

7 a. Derive the expressions for Z_{if} and Z_{of} for voltage series feedback connection type.

(06 Marks)

b. Draw the circuit diagram of uni-junction oscillator and explain the principle of operation and draw the characteristic curve. (08 Marks)

c. The following component values are given for the Wein-bridge oscillator of the circuit of $R_1 = R_2 = 33$ kΩ, $C_1 = C_2 = 0.001$ μb, $R_3 = 47$ kΩ, $R_4 = 15$ kΩ.

(i) Will this circuit oscillate?

(ii) Calculate the resonant frequency. (06 Marks)

OR

8 a. Briefly explain characteristics of negative feedback amplifier. (08 Marks)

b. Determine the voltage gain, input and output impedance with feedback for voltage series feedback having $A = -100$, $R_1 = 10$ kΩ and $R_0 = 20$ kΩ for feedback of $β = -0.1$. (04 Marks)

c. Explain characteristics of quartz crystal. With a neat diagram, explain the crystal oscillator in parallel resonant mode. (08 Marks)

Module-5

9 a. Explain series fed class A power amplifier. Show that its maximum conversion η is 25%.

(10 Marks)

b. For a class B amplifier providing a 20 V peak signal to a 16Ω load (speaker) and a power supply of $V_{CC} = 30$ V. Determine the input power, output power and circuit η. (10 Marks)

OR

10 a. Derive an expression for second harmonic distortion. (05 Marks)

b. Define voltage regulator. Explain the series voltage regulator using transistor. (08 Marks)

c. Derive an expression for conversion gain of class B push pull amplifier with neat circuit diagram and waveform. (07 Marks)

* * * * *