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10EE56

Fifth Semester B.E. Degree Examination, Aug. /Sept. 2020
Linear ICs and Application

Time: 3 hrs. Max. Marks:100

Note: *1. Answer FIVE full questions, selecting atleast TWO questions from each part.*
2. Missing data, if any, may be suitably assumed.

PART – A

1 a. Draw the circuit of a high Zin capacitor coupled voltage follower. Describe the circuit and design procedure. Drive an expression for the input resistance. **(10 Marks)**

b. Design a capacitor coupled inverting amplifier using a 741 op-amp and single polarity supply of +20V. The maximum input signal level is 50mV. The voltage gain is to be 68, and load resistance 500Ω. Draw the circuit diagram and show all values. **(06 Marks)**

c. Discuss upper cut-off frequency of an op-amp. Show how upper cut off frequency can be set for a non-inverting amplifier. **(04 Marks)**

2 a. Discuss the effect of the following on circuit stability
i) Stray capacitance
ii) Load capacitance
What are the means to counter instability caused by above? **(08 Marks)**

b. With suitable sketch explain :
i) Lag compensation network
ii) Lead compensation network
iii) Power supply decoupling
iv) Miller effect compensation. **(12 Marks)**

3 a. With a relevant diagram and waveforms describe the operation of a non – saturating precision half wave rectifier. **(07 Marks)**

b. Design a non – saturating precision half wave rectifier to produce a 2V peak output from a 1MHz sine wave input with a 0.5V peak value. Use a bipolar op – amp with a supply voltage of ±15V. **(04 Marks)**

c. Draw the circuit diagram (only) for the following (using op-amp)
i) Sample and hold
ii) Clamping circuit (clamp peak at zero)
iii) DAC using R – 2R ladder (3 bit). **(09 Marks)**

4 a. Draw an inverting Schmitt trigger circuit with different UTP and LTP explain the operation with suitable waveform, assuming input to be sinusoidal. **(08 Marks)**

b. Design a capacitor coupled ZCD using op-amp. The minimum signal frequency is 500Hz and max phase error acceptable is 3°. Supply voltage ±12V, draw the circuit diagram. **(06 Marks)**

c. Draw the circuit diagram of a monostable multivibrator and explain its operation with suitable waveforms. **(06 Marks)**

PART – B

5 a. Design a triangular waveform generator to produce a ±2V, 1KHz output. Use a ±15V supply. Specify minimum op-amp SR. draw the circuit diagram **(07 Marks)**

b. Design a phase shift oscillator to produce a 3KHz output frequency. The supply voltage is ±12V. Draw the circuit diagram, and indicate values of components. **(07 Marks)**

c. Draw the circuit diagram to provide control for adjusting the output amplitude and altering the DC voltage level of the output. **(06 Marks)**

6 a. Draw the circuit diagram of a second order low pass filter, sketch the gain frequency response and design equations. **(07 Marks)**

b. Design a Butterworth second order – high – pass filter circuit to have a cut off frequency of 6KHz. Calculate actual cut-off frequency for the selected component values. Draw circuit diagram. **(07 Marks)**

c. Design a single stage band – pass filter to have unity voltage gain and a pass band from 300Hz to 30KHz. Draw the circuit diagram. **(06Marks)**

7 a. Draw the circuit diagram of an universal active filter and explain its operation and design procedure. **(10 Marks)**

b. Draw the block diagram of a PLL and explain its operation. **(10 Marks)**

8 a. Draw the circuit diagram of an adjustable output voltage regulator. Discuss its operation and give design equations. **(10 Marks)**

b. Draw the circuit diagram and give explanation on the use of following IC voltage regulation.
– 723
– LM317
– LM337
– LM340
(10 Marks)

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