CBCS SCHEME

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17EE34

Third Semester B.E. Degree Examination, Aug./Sept.2020
Analog Electronic Circuits

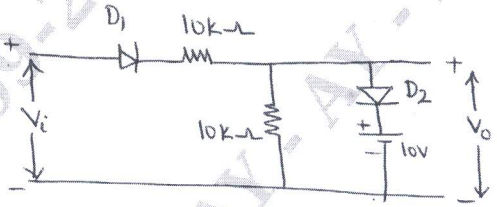
Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. For the clipper circuit shown in fig. Q1(a), the input is Vi = 50 Sinwt. Calculate and plot to scale the transfer characteristic, indicating slopes and intercept. **(10 Marks)**

Fig.Q1(a)



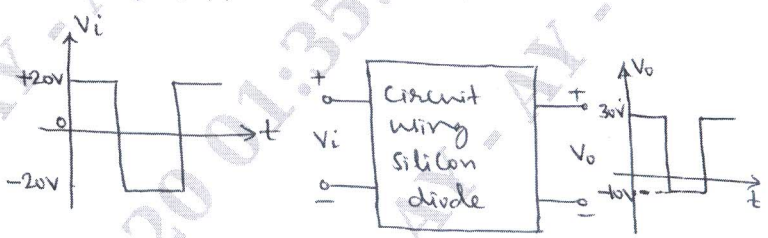
b. An emitter bias circuit has R_C = 2K Ω , R_E = 680 Ω , V_E = 2.1V, V_{CE} = 7.3V , I_B = 20μA. Find V_{CC}, R_B & β. **(05 Marks)**

c. What is meant by transistor biasing? Compare different biasing methods used for transistor biasing with respect to stability. **(05 Marks)**

OR

2 a. Design a suitable circuit represented by the box shown below. Which has input and output waveforms as indicated in fig. Q2(a). **(08 Marks)**

Fig.Q2(a)



b. Find the operating point for the voltage divider bias circuit with β = 80 and V_{BE} = 0.6V. Find the new operating point when β changes to 100 and V_{BE} changes to 0.25V. Given V_{CC} = 15V, R_1 = 100 KΩ , R_2 = 18KΩ , R_C = 4.7KΩ and R_E = 1KΩ. **(08 Marks)**

c. Explain the circuit of a transistor switch being used as an inverter. **(04 Marks)**

Module-2

3 a. Draw the hybrid small signal model of a transistor. Mention the advantages of h – parameters. **(04 Marks)**

b. Derive the expression for A_V, A_I, Z_i and Z_o for CE fixed bias configuration using complete hybrid equivalent model. **(10 Marks)**

c. State and prove Miller's theorem. **(06 Marks)**

OR

4 a. Derive the expressions for Z_i , Z_o , A_V and A_I for CB – configuration of transistor using approximate hybrid equivalent model. **(10 Marks)**

b. The circuit shown in fig.Q4(b) uses transistor with $h_{ie} = 1100\Omega$, $h_{fe} = 50$, $h_{oe} = 0.025 \times 10^{-3}$ ℧, $h_{re} = 2.5 \times 10^{-4}$. Calculate $R_i = \frac{V_1}{I_b}$, $R_i' = \frac{V_1}{I_1}$, $A_V = \frac{V_0}{V_1}$ and $A_{VS} = \frac{V_o}{V_S}$.

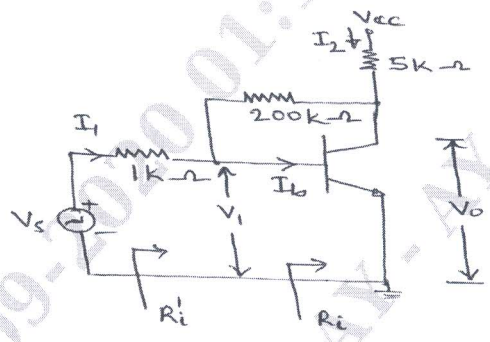


Fig.Q4(b)

(10 Marks)

Module-3

5 a. Explain with the help of circuit , what is cascade connection? What are the advantages of this connection? **(06 Marks)**

b. What is negative feedback in amplifiers? Show that negative feedback increases the bandwidth of an amplifier. **(08 Marks)**

c. An amplifier with negative feedback has a voltage gain of 100. It is found that without feedback , an input signal of 50mV is required to produce a given output. Where as with feedback the input signal must be 0.5V for the same output. Determine the value of A and β. **(06 Marks)**

OR

6 a. With appropriate h – parameters equivalent circuit , obtain the expression for Z_i, Z_o, A_v for a Darlington emitter follower. **(10 Marks)**

b. Derive expression Z_{if} and Z_{of} for voltage series feedback amplifier. **(10 Marks)**

Module-4

7 a. Discuss the different types of power amplifiers. **(04 Marks)**

b. Show that the maximum percentage efficiency for a series fed class A amplifier is 25%. **(10 Marks)**

c. A Quartz crystal has L = 0.12H , C = 0.04 PF , C_M = 1PF and R = 9.2 KΩ. Find i) f_s and ii) f_p. **(06 Marks)**

OR

8 a. State and explain the Barkhemsen's criterion to obtain sustained oscillations. **(06 Marks)**

b. With the help of circuit diagram, explain the working principle of R_c = phase shift oscillator, with relevant equations. **(08 Marks)**

c. A class B amplifier provides a 20V peak signal to a 16Ω load and a power supply of V_{CC} = 30V. Determine the input power, output power and circuit efficiency. **(06 Marks)**

Module-5

9 a. Draw the JFET amplifier using fixed bias configuration. Derive Z_i, Z_o and A_v using small signal model. **(08 Marks)**

b. Compare JFET and MOSFET. **(04 Marks)**

c. Design a fixed bias circuit of fig. Q9(c) to have ac gain of -15. Calculate the value of R_D to get this gain , if $V_{DD} = 40V$, $R_G = 10m\Omega$, $I_{DSS} = 10mA$, $V_P = -4V$, $Y_{OS} = 20\mu s$, $C_1 = 0.1\mu F$. **(08 Marks)**

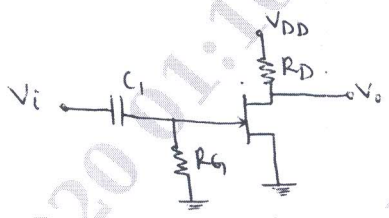


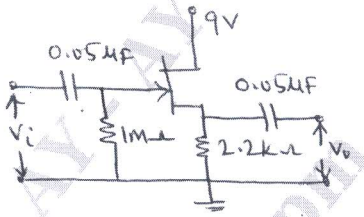
Fig.Q9(c)

OR

10 a. Sketch a typical characteristics for an n – channel JFET. Explain the shape of the characteristics and identify the regions. **(10 Marks)**

b. Calculate the voltage gain , input and output impedance for the circuit of fig. Q10(b). Given $I_{DSS} = 16mA$, $V_P = -4V$, $r_d = 40K\Omega$, $V_{GSO} = -2.86V$. **(10 Marks)**

Fig.Q10(b)



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