CBCS SCHEME

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15EE35

Third Semester B.E. Degree Examination, Aug./Sept.2020
Digital System Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define combinational logic. List the various steps in designing combinational logic system. **(05 Marks)**

b. Simplify the following expression using K-map and implement using basic gates, $f(a, b, c, d) = \sum m(0, 1, 2, 5, 6, 7, 8, 9, 10) + d(13, 14, 15)$. **(06 Marks)**

c. Find the minimal sum using MEV technique with a, b, c as map variables for the given function $f(a, b, c, d) = \sum(3, 4, 5, 7, 8, 11, 12, 13, 15)$ **(05 Marks)**

OR

2 a. Explain canonical minterm form and maxterm form expressions with examples. **(04 Marks)**

b. Express the following Boolean expression into minterm canonical form $f(w, x, y, z) = (w' + x)(y + z)$ **(04 Marks)**

c. Obtain all the prime implicants of the following function using Quine-Mccluskey method $f(a, b, c, d) = \sum(0, 2, 3, 5, 8, 10, 11)$ **(08 Marks)**

Module-2

3 a. Distinguish between decoder and encoder. **(03 Marks)**

b. Implement the following function using 3 to 8 line decoder with active low output and explain implementation $f(a, b, c) = a\bar{b} + bc$ **(07 Marks)**

c. Implement the expression $y = ad + b\bar{c} + bd$ using 8:1 MUX with least significant bits as select inputs. **(06 Marks)**

OR

4 a. Implement full adder circuit using 74153 4:1 MUX. **(06 Marks)**

b. Explain 4-bit parallel adder with block diagram. **(04 Marks)**

c. Design a two-bit binary comparator using logic gates. **(06 Marks)**

Module-3

5 a. What is a Flip-Flop? Explain the working of edge triggered D Flip-Flop with its functional table. **(08 Marks)**

b. Design a synchronous Mod-6 counter using clocked JK Flip-Flop. **(08 Marks)**

OR

6 a. Explain the working of pulse triggered J-K Master-slave Flip-Flop with its logic symbol and truth table. **(08 Marks)**

b. What is meant by universal shift register? Explain the principle of operation of 4-bit universal shift register. **(08 Marks)**

Module-4

7 a. Explain Mealy Model for a clocked sequential circuit. **(06 Marks)**

b. For the state diagram shown in Fig.Q.7(b), write the excitation table and state table with R.S. Flip-Flop. **(05 Marks)**

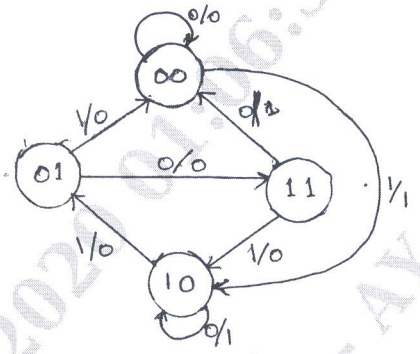

Fig.Q.7(b)

c. Write the step-by-step procedure for the design of clocked synchronous sequential circuit. **(05 Marks)**

OR

8 a. Explain Moore model for a synchronous sequential circuit. **(06 Marks)**

b. Give the output function, transition table and state diagram by analyzing the sequential circuit shown in Fig.Q.8(b) **(10 Marks)**

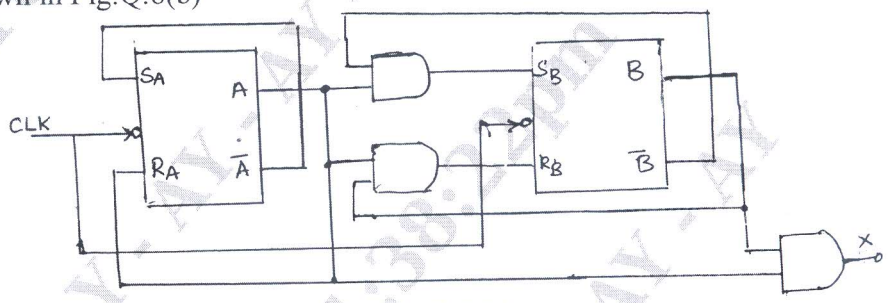

Fig.Q.8(b)

Module-5

9 a. Explain the structure of VHDL module. **(04 Marks)**

b. Mention the types of HDL descriptions. Explain dataflow and behavioral descriptions. **(06 Marks)**

c. Write a dataflow description for a full adder with active high enable, in both VHDL and verilog module. **(06 Marks)**

OR

10 a. If A, B, C are three unassigned variables with A = 11110000, B = 01011101, C = 00000000 find the value of

i) A NAND B ii) A && C iii) ~1B iv) A rov 2 v) ! B **(05 Marks)**

b. List the data types classification VHDL. Mention advantages of VHDL data types over verilog. **(06 Marks)**

c. Give comparison between VHDL and verilog. **(05 Marks)**

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