CBCS SCHEME

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18EE35

Third Semester B.E. Degree Examination, Aug./Sept.2020
Digital System Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. With a basic block diagram, explain the combinational logic circuit. **(04 Marks)**

b. Convert the following in the proper canonical formula and write the decimal notation.

i) $R = f(x, y, z) = (x + y)(\bar{x} + z)$ into maxterm canonical formula

ii) $Z = f(a, b, c) = ab + \bar{b}c + ac$ into minterm canonical formula. **(08 Marks)**

c. Reduce the following expression using k map and implement using basic gates.

i) $f(a, b, c, d) = \Sigma m(0, 1, 2, 3, 8, 9)$

ii) $f(A, B, C, D) = \pi M(0, 1, 4, 5, 14, 15) + d(12, 13)$. **(08 Marks)**

OR

2 a. Find the minimal sum and minimal product expression for the function :

$f(a, b, c, d) = \Sigma m(4, 5, 12, 13, 14, 15) + d(10,11)$. **(06 Marks)**

b. Simplify using Quine Mc Cluskey method :

$f(a, b, c, d) = \Sigma m(0, 2, 8, 10)$. **(07 Marks)**

c. Simplify using k Map.

$f(a, b, c, d, e) = \Sigma m(0, 1, 2, 3, 4, 5, 16, 17, 18, 19, 24, 25) + d(26, 27)$. **(07 Marks)**

Module-2

3 a. Design a 3 inputs, a, b and c and output y combinational circuit which has an output equal to 1 when majority of its inputs equal to 1 and output is 0 otherwise. **(06 Marks)**

b. Design a full adder by constructing the truth table and simplify the output equations. **(06 Marks)**

c. Implement the function :

$f(a, b, c, d) = \Sigma m(4, 5, 7, 9, 11, 12, 13, 15)$

using :

i) 8 : 1 MUX with a, b, c, as select lines

ii) 4 : 1 MUX with a, b as select lines. **(08 Marks)**

OR

4 a. What is a Comperator? Design a 2 bit magnitude comperator using logic gates. **(10 Marks)**

b. Implement the following multiple function using one 74LS138 and external gates.

$f_1(A, B, C) = \Sigma m(1, 3, 4, 6)$

$f_2(A, B, C) = \pi M(2, 3, 5, 7)$. **(06 Marks)**

c. Configure a 16 : 1 MUX using 4 : 1 MUX. **(04 Marks)**

Module-3

5 a. Explain the operation of Master – Slave JK flipflop with logic diagram, truth table, symbol and timing diagram. **(10Marks)**

b. Differentiate latches and flipflops. Derive the characteristic equation of SR flipflop, JK flipflop, T flipflop and D flipflop. **(10 Marks)**

OR

6 a. Explain the operation of a Gated SR Latch using NAND logic. **(08 Marks)**

b. Explain the working of a switch debouncer using SR Latch with wave forms. **(08 Marks)**

c. Convert a JK flipflop to T flipflop. **(04 Marks)**

Module-4

7 a. Differentiate synchronous and asynchronous counter. **(04 Marks)**

b. Design a Mod 10 ripple counter using JK flipflop. **(06 Marks)**

c. Draw the logic diagram of a 4 bit shift register with four D flipflop and four 4 : 1 MUX with mode select inputs S_1 and S_0. The resister operates as follows :

S_1	S_0	Register Operation
0	0	No change
0	1	Compliment
1	0	Clear to zero
1	1	Load parallel data

(10 Marks)

OR

8 a. Mention the four different modes of operation shift register. With a neat block diagram, explain the operation of a 4 bit ring counter and Johnson counter. **(10 Marks)**

b. Design a MOD6 synchronous upcounter using T flipflop. **(10 Marks)**

Module-5

9 a. With a neat block diagram, explain and distinguish between Moore and Mealy model in a sequential circuit analysis. **(10 Marks)**

b. Design a synchronous counter using JK flipflop to count the following sequence :
$7 \rightarrow 4 \rightarrow 3 \rightarrow 1 \rightarrow 6 \rightarrow 0 \rightarrow 7$. **(10 Marks)**

OR

10 a. What are the different types of RAM and ROM? Explain. **(10 Marks)**

b. Construct a sequential circuit by obtaining the state and excitation table for the given diagram using KJ flipflop.

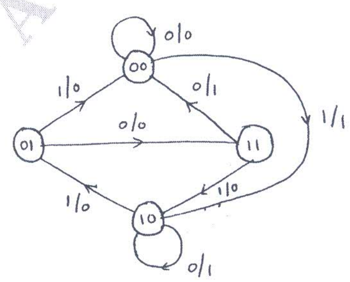

Fig.Q10(b) **(10 Marks)**

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