CBCS SCHEME

USN | | | | | | | | | |

15EE34

Third Semester B.E. Degree Examination, Aug./Sept.2020
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 80

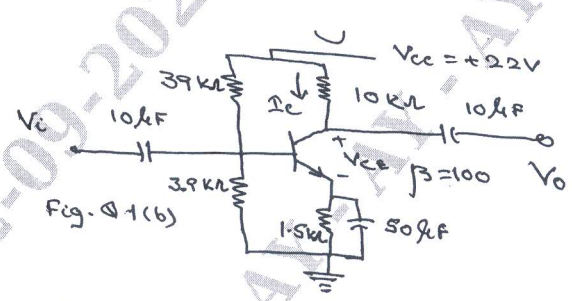
Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define Clamper. Explain operation of a negative clamper, with a diagram. **(05 Marks)**

b. Determine dc bias voltage V_{CE} and current I_C for the network shown in fig. Q1(b) using exact analysis. **(05 Marks)**

Fig. Q1(b)

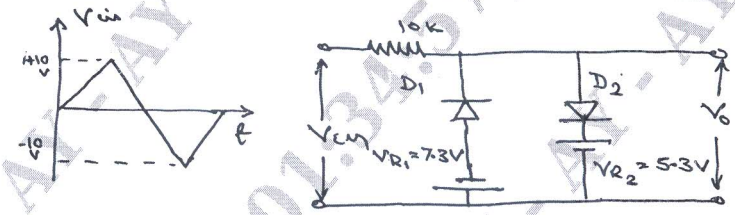


c. Define Stability factors of a transistor. Derive expressions for $S(I_{CO})$ and $S(V_{BE})$ for Fixed Bias Circuit. **(06 Marks)**

OR

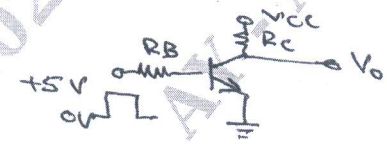
2 a. For the circuit shown in fig. 2(a) sketch output waveform and transfer characteristic for cut in voltage = 0.7V. **(08 Marks)**

Fig. Q2(a)



b. Explain functioning of transistor switch circuit. Calculate resistor R_B value that saturates the transistor switch when $V_i = +5V$, $R_c = 1K$, $\beta = 100$, $V_{CC} = +5V$ and $V_{CE_{sat}} = 0.2V$.

Fig. Q2(b)



(08 Marks)

Module-2

3 a. Draw AC equivalent circuit with r_e model for a CE amplifier with voltage divider biasing and derive expressions for voltage gain, current gain , input and output impedances. **(08 Marks)**

b. Describe factors that affect low frequency response of a BJT CE amplifier. Derive expressions for lower cut off frequencies due to C_S , C_C and C_E capacitances. **(08 Marks)**

OR

4 a. Explain Hybrid equivalent model for a transfer. Draw h – parameter models for CE and CB configurations. **(05 Marks)**

b. Derive expressions for Miller input ($CM_i = (1 - AV)\, C_f$) and Miller output capacitance ($CM_O = (1 - \frac{1}{AV})\, C_f$). **(06 Marks)**

c. Define f_α , f_β and f_T and state relation between f_β and f_T. (05 Marks)

Module-3

5 a. What is CASCODE connection / configuration? List important characteristics. (05 Marks)

b. Explain the four types of feedback connections. Give one example of a practical feedback circuit. (06 Marks)

c. Determine Voltage gain, Input and Output impedances with feedback for a voltage series feedback circuit having $A = -100$, $Z_i = 10k\Omega$, $Z_o = 20\ k\Omega$ with $\beta = -0.1$. (05 Marks)

OR

6 a. For the Cascaded arrangement shown in fig.Q6(a), calculate loaded gains for each stage, total gains AV_T, AV_S , total current gain AI_T and phase relationship between V_i and V_o.

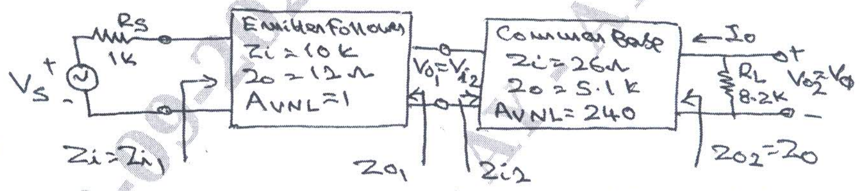


Fig. Q6(a) (08 Marks)

b. With an equivalent circuit diagram for a Darlington Emitter follower, derive expressions for Z_{in} , A_I , Z_O and A_V. (08 Marks)

Module-4

7 a. Derive expression for conversion efficiency of Transformed Coupled Class A Power amplifier. (06 Marks)

b. Calculate harmonic distortion components and Total Harmonic distortion for an output signal having Fundamental amplitude of 2.5V , Second harmonic amplitude of 0.25V , Third harmonic amplitude of 0.1V and Fourth harmonic amplitude of 0.05V. (05 Marks)

c. Explain basic principle of oscillators and effect of loop gain ($A\beta$) on output of oscillator. (05 Marks)

OR

8 a. Draw the circuit of class B push pull power amplifier and explain operation with neat input and output wave forms. (08 Marks)

b. Draw circuit diagram of RC phase shift oscillator and derive expression for the frequency of operation. (08 Marks)

Module-5

9 a. Compare BJT with FET. (05 Marks)

b. Determine V_{GSQ} ,T_{DQ} and V_{DS}, V_D for circuit shown in fig. Q9(b). (06 Marks)

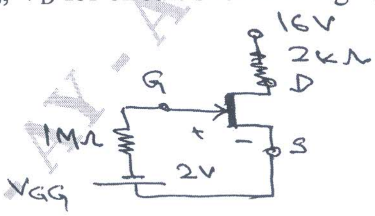


Fig. Q9(b)

c. Explain working of n – channel Enhancement MOSFET, with neat diagram. (05 Marks)

OR

10 a. With the help of Small signal model, derive expressions for Voltage gain, input and output impedances of a common source JFET amplifier with Fixed bias. (08 Marks)

b. Explain Construction and Operation of n – channel Depletion type MOSFET. Draw the characteristics. (08 Marks)