



CBCS SCHEME

15CS72

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Seventh Semester B.E. Degree Examination, Aug./Sept.2020 Advanced Computer Architectures

Time: 3 hrs.

Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. With a neat diagram. Describe the three shared memory multi processor models. (06 Marks)
- b. Determine the parallel pairs for the following program statements and prove that parallel processing will yield highest performance compared to sequential processing.
- P1 : $C = D \times E$
P2 : $M = G + C$
P3 : $A = B + C$
P4 : $C = L + M$
P5 : $F = G / E$ (05 Marks)
- c. Explain any five basic metrics affecting the scalability of a computer system for a given application. (05 Marks)

OR

- 2 a. With respect to dependencies between the instructions, discuss the following with example:
- i) Data dependency
ii) Control dependency
iii) Resource dependency (06 Marks)
- b. Explain the different levels of parallelism. (06 Marks)
- c. Write note on Amadahl's Law. (04 Marks)

Module-2

- 3 a. Differentiate the characteristics of CISC and RISC Architecture. (06 Marks)
- b. Explain the architectural features of VLIW processor with timing diagram. How does it differ from superscalar processor? (10 Marks)

OR

- 4 a. List the symbolic processor characteristics. Explain the architecture of symbolic 3600 LISP processor. (08 Marks)
- b. With a neat diagram, explain memory hierarchy from low to high levels in detail. (08 Marks)

Module-3

- 5 a. Explain synchronous and Asynchronous bus timing protocols. (05 Marks)
- b. Explain the features of nonlinear pipeline processor with feed forward and feed backwards connections. (05 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

- c. Consider the following reservation table for a 4-stage pipeline with a clock cycle $\tau = 2ns$.

	1	2	3	4	5	6
S ₁	X					X
S ₂		X		X		
S ₃			X			
				X	X	

- What are the forbidden latencies and the initial collision vector?
- Draw the state transition diagrams for scheduling the pipeline.
- Determine the MAL associated with shorted greedy cycle.
- Determine the pipeline throughput corresponding to the MAL and given τ .
- Determine the lower bound on the MAL for this pipeline, have you obtained the optimal latency from the above state diagram.

(06 Marks)

OR

- With state diagrams, explain the state transition diagram for a pipeline unit. (05 Marks)
- Explain the Tomasulo's algorithm for dynamic instruction scheduling. (05 Marks)
- Consider the following pipeline reservation table:

	1	2	3	4
S ₁	X			X
S ₂		X		
S ₃			X	

- What are the forbidden latencies?
- Draw the state transition diagram.
- List all the simple cycles and greedy cycles.
- Determine the optimal constant latency cycle and the minimal average latency.
- Let the pipeline clock period be $\tau = 20ns$. Determine the throughput of this pipeline.

(06 Marks)

Module-4

- With a neat diagram, explain the bus systems at board level, back plane and I/O level. (08 Marks)
- Define cache coherence problem. Describe cache coherence problems in data sharing and process migration. (08 Marks)

OR

- Explain Goodman's write once cache coherence protocol using write invalidate policy on write back caches. (08 Marks)
- With a neat diagram, explain C-access and S-access organization for an m-way interleaved memory. (08 Marks)

Module-5

- With a neat sketch, explain the compilation phases in parallel code-generation. (08 Marks)
- Discuss in brief difference between local and global branch prediction and how a 2 bit branch selector may be used per branch to select between two. Explain with transition diagram. (08 Marks)

OR

- Explain the different loop transformations and discuss how to apply to them for loop vectorization or parallelism. (08 Marks)
- Describe in brief the structure of the reorder buffer and how the use of reorder buffer addresses the various types of dependences in the program. (08 Marks)

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