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18CS34

Third Semester B.E. Degree Examination, Aug./Sept.2020
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. With a neat diagram, analyze the basic operational concepts of a computer. Give the operating steps. **(10 Marks)**

b. Analyze Big Endian and Little Endian methods of byte addressing with proper example. **(05 Marks)**

c. Explain SPEC rating of computer. **(05 Marks)**

OR

2 a. What is an Addressing mode? Explain any four types of addressing modes, with suitable example. **(10 Marks)**

b. What is a Subroutine? Analyse the use of call (or) Return Instructions in a subroutine with assembly language program code. **(10 Marks)**

Module-2

3 a. With neat sketches, explain various methods for handling multiple Interrupts requests raised by Multiple devices. **(10 Marks)**

b. What is DMA Bus Arbitration? Briefly explain different bus arbitration techniques. **(10 Marks)**

OR

4 a. Explain Synchronous Bus and Asynchronous Bus with neat Timing diagrams. **(10 Marks)**

b. Enumerate the features of Universal Serial Bus. **(05 Marks)**

c. Describe how a read operation is performed in a PCI bus. **(05 Marks)**

Module-3

5 a. With a neat diagram, explain the Internal Organization of 128 × 8 memory chip. **(10 Marks)**

b. Describe the working of Static RAM memories. **(05 Marks)**

c. Analyze the working mechanism of Asynchronous DRAMS. **(05 Marks)**

OR

6 a. Analyze how data are written into Read Only Memories (ROM). Discuss different types of Read Only Memories. **(10 Marks)**

b. What is Cache memory? Analyze the three mapping functions of Cache memory. **(10 Marks)**

Module-4

7 a. Design a logic circuit to perform addition and subtraction of two 'n' – bit numbers X and Y. This circuit can be suitably modified to perform Y – X operation. **(08 Marks)**

b. Design an 'n' bit carry propagation adder circuit to add 'K' – 'n' bit numbers. **(07 Marks)**

c. Subtract – 5 from -7 using Two's complement subtraction. **(05 Marks)**

OR

8 a. Analyze the design of Carry Look Ahead adder circuit suitable logic circuit diagram. **(10 Marks)**

b. Explain Booth Multiplication Algorithm. Apply Booth Multiplication Algorithm to multiply the signed number – 5 and 4. **(10 Marks)**

Module-5

9 a. Explain the working of single bus organization of data path. **(07 Marks)**

b. Write the sequence of control steps to execute the Instruction Add (R_3) , R_1 on single bus architecture. **(05 Marks)**

c. Analyze how does execution of a complete instruction carry out. **(08 Marks)**

OR

10 a. What is the purpose of Control unit? With neat sketches, explain the organization of Hardwired control unit in detail. **(10 Marks)**

b. What is Pipelining? Explain the five stage Instruction pipeline with timing diagram. **(10 Marks)**

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