CBCS SCHEME

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17CS/IS34

Third Semester B.E. Degree Examination, Aug./Sept.2020
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Draw the connection between the processor and memory. Elaborate the functions of each component in the connection. **(07 Marks)**

b. Write the basic operational steps needed to execute the machine instruction "Add LOCA, R0". **(05 Marks)**

c. What is a stack frame? Explain a commonly used layout for information in a subroutine stack frame. **(08 Marks)**

OR

2 a. Write the Register Transfer Notation for the following instructions: (i) MOV LOC, R1 (ii) Add R1, R2, R3 **(02 Marks)**

b. Define Addressing Modes. Explain the following addressing modes with suitable examples: (i) Register (ii) Direct (iii) Indirect (iv) Index (v) Auto-decrement **(12 Marks)**

c. Write an assembly program to add N numbers stored in a consecutive memory location as NUM_1, NUM_2,....., NUM_n and store the result at location SUM by using the branching technique. **(06 Marks)**

Module-2

3 a. What do you mean by DMA? Explain its operation using registers in a DMA interface. **(08 Marks)**

b. Define Bus arbitration. Explain the two types of bus arbitration. **(12 Marks)**

OR

4 a. Explain the I/O interface for an input device (keyboard interface) to the processor with a neat block diagram. **(08 Marks)**

b. Summarize the working mechanism of SCSI bus, and its controllers. Discuss the main phases involved during the read operation using SCSI bus. **(08 Marks)**

c. Differentiate between serial and parallel port communication. **(04 Marks)**

Module-3

5 a. Discuss the read and write operation in a single SRAM cell with the help of circuit diagram. **(05 Marks)**

b. Show the working of a single transistor DRAM cell with the circuit diagram and list its advantages. **(05 Marks)**

c. What is cache memory? Explain the direct and associative mapping techniques. **(10 Marks)**

OR

6 a. Draw and discuss the organization of 1K × 1 memory chip. **(05 Marks)**

b. Design a memory organization of a 2M × 32 memory module using 512K × 8 static memory chips and explain the same. **(06 Marks)**

c. Explain the virtual memory organization and its address translation mechanism using paging technique. **(09 Marks)**

Module-4

7 a. Convert the following pairs of decimal numbers to 5-bit, signed, 2′ S-complement, binary numbers and add them. State whether or not overflow occurs in each case.
(i) 5, 10 (ii) −14, 11 (iii) −3, −8 (iv) −10, −13 **(10 Marks)**

b. Describe the principle of Carry-Look Ahead Addition for a 4-bit adder circuit, built using B-cells and calculate the number of gate delays for S_3 and C_4. **(10 Marks)**

OR

8 a. Perform the division operation for 11 ÷ 2 using (i) Restore (ii) Non-restore methods. **(10 Marks)**

b. Write the process of assigning weights for bit-pair recoding of multipliers for achieving fast multiplication in case of signed numbers. **(05 Marks)**

c. Find the product of +13 and −6 using the bit-pair recoding of multiplier technique. **(05 Marks)**

Module-5

9 a. Show a possible control sequence for execution of a complete instruction Add (R_3), R_1 on a single bus processor. **(07 Marks)**

b. Describe the three-bus organization of data path with a neat diagram. **(08 Marks)**

c. With a neat block diagram, explain the working principles of a digital camera. **(05 Marks)**

OR

10 a. Explain the three possible ways of implementing a multiprocessor system using MIMD architecture. **(12 Marks)**

b. Write short notes on:
(i) Hardwired Control
(ii) Micro programmed Control **(08 Marks)**

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