CBCS SCHEME

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17CS/IS32

# Third Semester B.E. Degree Examination, Aug./Sept. 2020
## Analog & Digital Electronics

Time: 3 hrs. Max. Marks: 100

**Note:** ***Answer any FIVE full questions, choosing ONE full question from each module.***



### Module-1

1 a. With circuit symbol and characteristic curves, explain the working of N-Channel E-MOSFET. **(08 Marks)**

b. List out the differences between JFETs and MOSFETs. **(06 Marks)**

c. Briefly discuss the working principles of CMOS. **(06 Marks)**

**OR**

2 a. Explain with a neat diagram current to voltage and voltage to current converter (using opamp) **(06 Marks)**

b. Explain the performance parameter of opamp. **(08 Marks)**

c. With necessary circuit diagram and waveforms, explain the operation of a relaxation oscillator using opamp. **(06 Marks)**

### Module-2

3 a. Give simplified logic equation of $y = \sum m(0,1,2,3,10,11,12,13,14,15)$ using Quine-Mc clusky method. **(10 Marks)**

b. Find the minimal sum and minimal product using K-map.
$f(a,b,c,d) = \sum m(6,7,9,10,13) + d(1,4,5,11)$ **(08 Marks)**

c. Implement the following using NAND gates only. **(02 Marks)**

**OR**

4 a. Draw the timing diagram and write a verilog HDL code (using structural model) for the Boolean function Y = NAND ($y_1$, $y_2$) where $y_1 = A + B$ and $y_2 = B + C$. **(08 Marks)**

b. Write the truth table of the logic circuit having three inputs A, B and C and the output expression as $y = \overline{A}BC + ABC$. Also simplify the expression using Boolean algebra and implement the logic circuit using NAND gates. **(06 Marks)**

c. Realize basic gates using only NAND gates and only NOR gates. **(06 Marks)**

### Module-3

5 a. Implement the following Boolean function using 4 : 1 MUX.
$F(A, B, C, D) = \sum m(0,1,2,4,6,9,12,14)$ **(06 Marks)**

b. Construct 16 : 1 MUX using 4 to 1 and 2 to 1 MUX. **(06 Marks)**

c. What is magnitude comparator? Design and explain 2-bit magnitude comparator. **(08 Marks)**

**OR**

6 a. Explain the positive edge-triggered JK flip flop with necessary logic diagram, truth table and waveforms. **(08 Marks)**

b. Illustrate the three basic circuits used in arithmetic building blocks. **(06 Marks)**

c. Design a 4 to 1 MUX, using conditional assign and case statements. **(06 Marks)**

## Module-4

7 a. Briefly discuss the various representations of flip flops. **(12 Marks)**

b. Explain parallel-in-serial out shift register with example. **(08 Marks)**

**OR**

8 a. With block diagram, truth table and output waveforms, explain the 3-bit binary ripple down counter. **(10 Marks)**

b. Design synchronous mod-5 up counter using JK flip flops. **(10 Marks)**

## Module-5

9 a. Design and construct divide by 60 counter. **(10 Marks)**

b. Design a self-correcting modulo-6 counter in which all unused state leads to state CBA = 000. **(10 Marks)**

**OR**

10 a. With n7ecessary circuit diagram and waveform, explain continuous analog-to-digital converter. **(10 Marks)**

b. Explain 4-bit digital to analog converter. **(10 Marks)**

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