CBCS SCHEME

USN | LAY14MT046 | 15MT62

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Embedded System (ARM)

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. What is meant by ARM.? List out steps present in ARM design philosophy. **(08 Marks)**

b. Describe the following :
i) Generic program status register
ii) Processor modes. **(08 Marks)**

OR

2 a. Explain the following embedded system hardware components :
i) ARM Bus technology
ii) ARM Bus protocol
iii) Memory. **(08 Marks)**

b. Explain pipeline concept in detail. **(08 Marks)**

Module-2

3 a. Explain the following instruction with syntax :
i) Logical instruction
ii) Comparison instruction. **(08 Marks)**

b. Software incorrupt instruction write example with pre and post condition. **(08 Marks)**

OR

4 a. Explain the thumb load store instruction using :
i) Single register
ii) Multiple register syntax. **(08 Marks)**

b. Explain the following thumb instruction :
i) ARM–thumb interworking
ii) Multiple register Load-store instruction example. **(08 Marks)**

Module-3

5 Describe the following load scheduling process :
a. Load scheduling by preloading
b. Load scheduling by unrolling. **(16 Marks)**

OR

6 a. Making the most of available register in register allocation with count shift example. **(08 Marks)**

b. Describe bit manipulation concept in short. **(08 Marks)**

Module-4

7 a. Explain the following cache policy :
   i) Write policy
   ii) Cache line replacement polices
   iii) Allocation policy on a cache miss. (08 Marks)

b. Draw main memory maps to a direct mapped cache in cache architecture. (08 Marks)

OR

8 Describe the following concept in cache lockdown.
   a. Locking a cache by incrementing the way
   b. Locking a cache using lock bits. (16 Marks)

Module-5

9 Write following concept with neat description :
   a. Assigning interrupts
   b. Interrupt latency
   c. IRQ and FIQ exception. (16 Marks)

OR

10 Explain the following :
   a. Non nested interrupt handler
   b. Nested interrupt handler
   c. Prioriszed simple interrupt handler. (16 Marks)

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