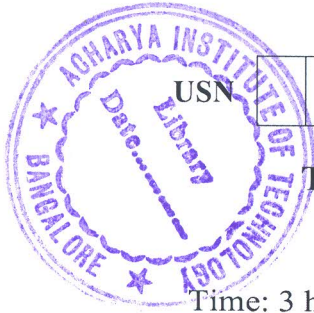


CBCS SCHEME



USN

--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

18MT36

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020 Computer Organization and Architecture

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain with a neat diagram, the connection between processor and computer memory and also typical operating steps for executing an instruction. (10 Marks)
- b. Write the basic performance equation. Explain the role of each of the parameter in the equation. (05 Marks)
- c. Explain Big-endian and Little-endian method with neat diagram. (05 Marks)

OR

- 2 a. List and explain three system used for representing signed numbers. (05 Marks)
- b. What is straight line sequencing? Explain with example program. (05 Marks)
- c. What are the basic instruction types? Explain with example. (10 Marks)

Module-2

- 3 a. Define addressing mode. Explain various addressing modes with example. (10 Marks)
- b. What is parameter passing? How are parameters passed to subroutine using registers? (05 Marks)
- c. What is stack? Write a routine for safe push operation and safe pop operation. (05 Marks)

OR

- 4 a. Explain logical shift and rotate operations with example. (10 Marks)
- b. What are assembler directives? Explain assembler directives with example program. (10 Marks)

Module-3

- 5 a. Discuss the different schemes available to enable and disable interrupts. (06 Marks)
- b. What is interrupt nesting? Explain with a neat diagram, the implementation of interrupt priority using individual interrupt request and acknowledge lines. (08 Marks)
- c. Explain how simultaneous interrupt request from several I/O devices will be handled by a processor through a single INTR line. (06 Marks)

OR

- 6 a. What is DMA? With a neat diagram, discuss how DMA controller registers accessed by the processor to initiate transfer operations. (08 Marks)
- b. What is memory mapped I/O? Explain I/O interface for an input device with a neat diagram. (06 Marks)
- c. What is interrupt? Explain transfer of control through the use of interrupts? (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and/or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-4

- 7 a. Draw the organization of $1K \times 1$ memory chip and explain its working. (08 Marks)
b. Draw and explain the working of single transistor dynamic memory cell. (06 Marks)
c. Define ROM. List and explain various types of ROMs. (06 Marks)

OR

- 8 a. What is virtual memory? Explain virtual memory organization with a neat diagram. (06 Marks)
b. Explain the following with respect to cache memory :
i) Write through protocol
ii) Write back protocol
iii) Load-through approach. (06 Marks)
c. Explain the internal organization of $2m \times 8$ dynamic memory chip with a neat diagram. (08 Marks)

Module-5

- 9 a. Explain single bus organization of datapath with a neat block diagram. (06 Marks)
b. Explain the hardwired control unit organization in a processing unit. (08 Marks)
c. Write the control sequence for instruction execution for Add (R3), R1 in the execution of a complete instruction. (06 Marks)

OR

- 10 a. Explain the micro-programmed control unit organization in a processing unit. (08 Marks)
b. How a word is fetched from memory? Explain the connection and control signals for MDR register with a neat diagram. (08 Marks)
c. Write a control sequence for the execution of the instruction add R4, R5, R6 in three bus organizations. (04 Marks)
